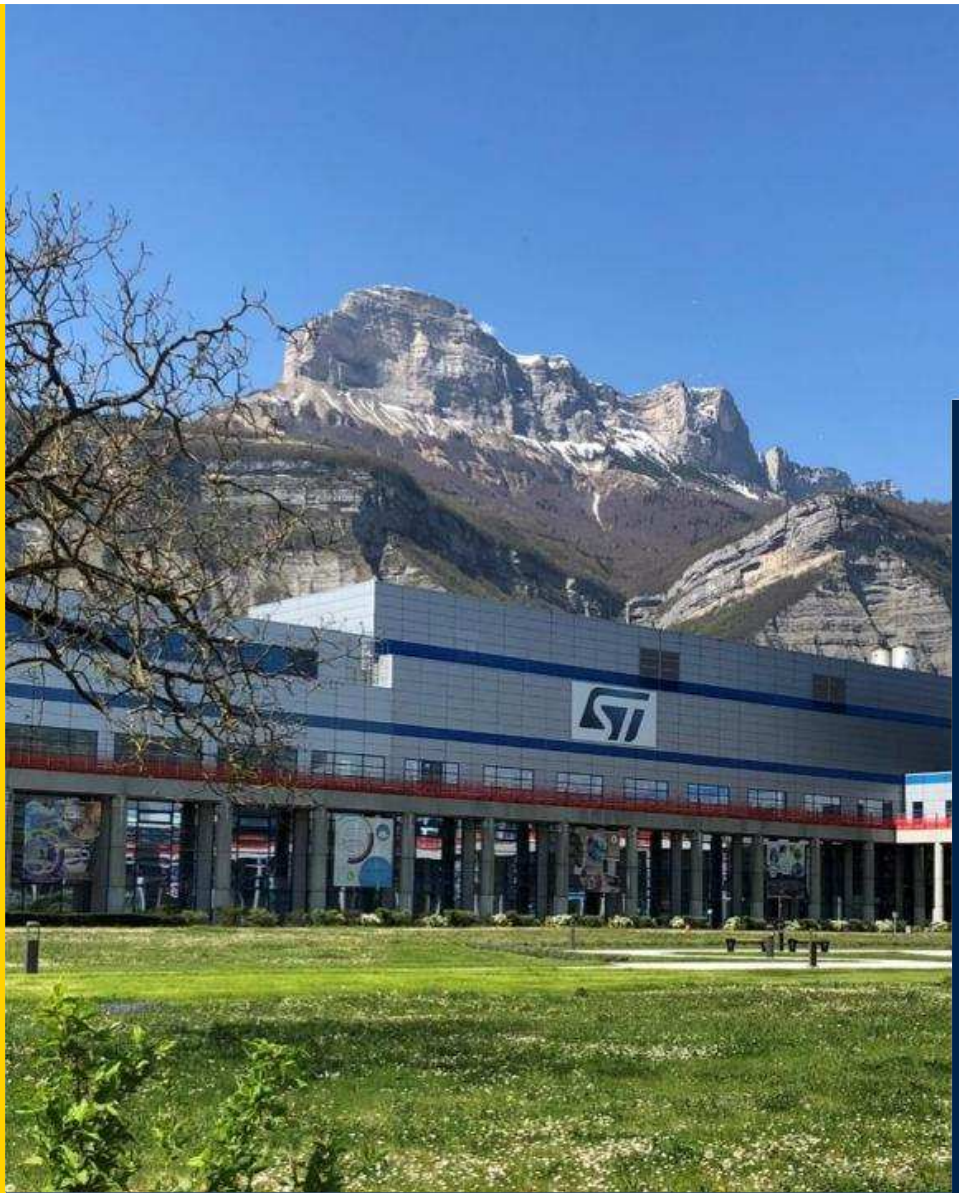

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# New reliability challenges for 3D integration stacking using hybrid bonding

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*** Member of Technical Staff**
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# Driving forces for new devices


Reduced cost

Form factor

Increase functionalities

Performance

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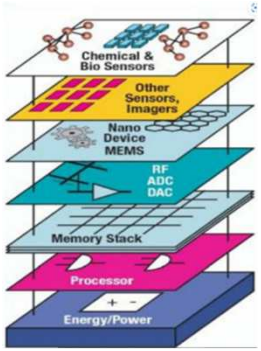
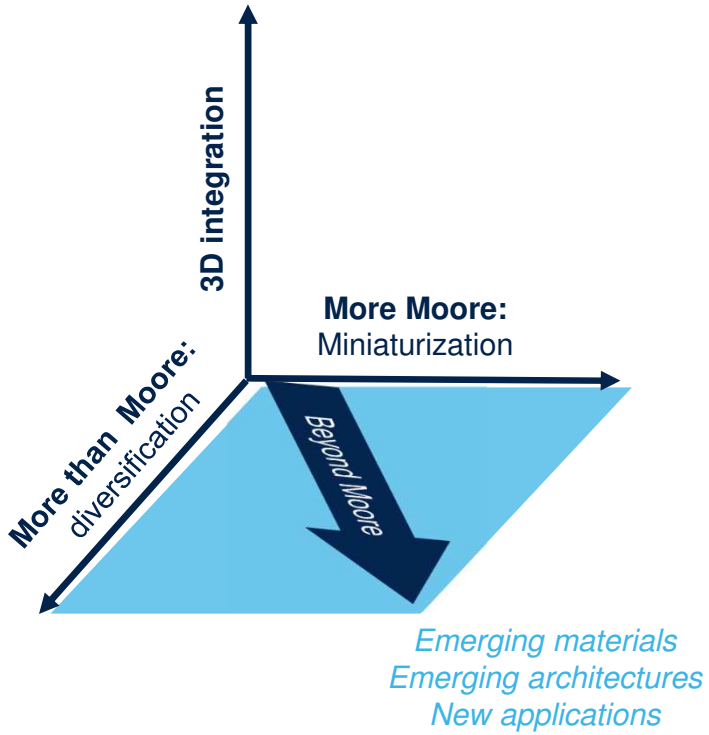
# Going beyond the limits of integration




J.-Q. Lu, FUTURE FAB International, Issue 41, 2012




- '**Beyond Moore:** an approach seeking to achieve the best of both More Moore and More than Moore worlds, and the key to doing so is advanced heterogeneous integration.
- **Hybrid bonding stacking** being the most scalable 3D integration is a major enabler for More than Moore and will play a determinant role for Beyond CMOS developments

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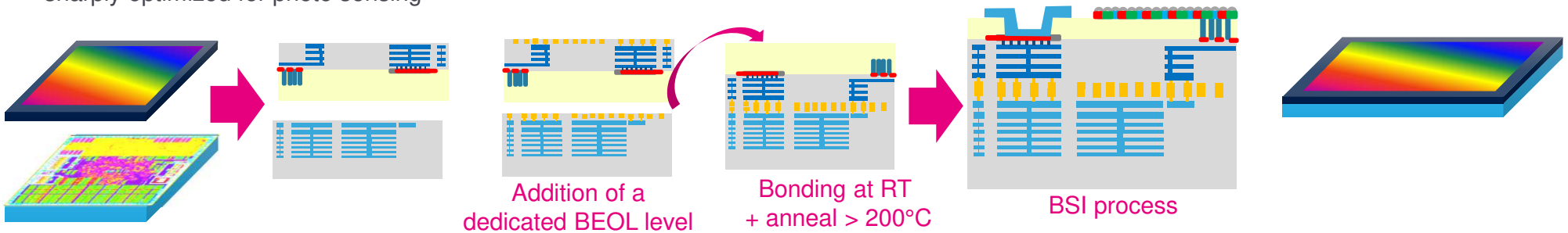
# 3D stacking using hybrid bonding

## Massive performant and new functionalities booster for Image Sensor

**Photo-site array**
► Dedicated technology, sharply optimized for photo sensing

**Pixel BS dedicated technology**
► Pixel with high dynamic & low noise
► High QE, including in NIR




**Low power processor**
► Low noise analog and high speed, low power, digital imaging

**Advanced Digital & Analog CMOS**
► Digital with high density & low power

**Dedicated layers introduced to enable hybrid bonding**

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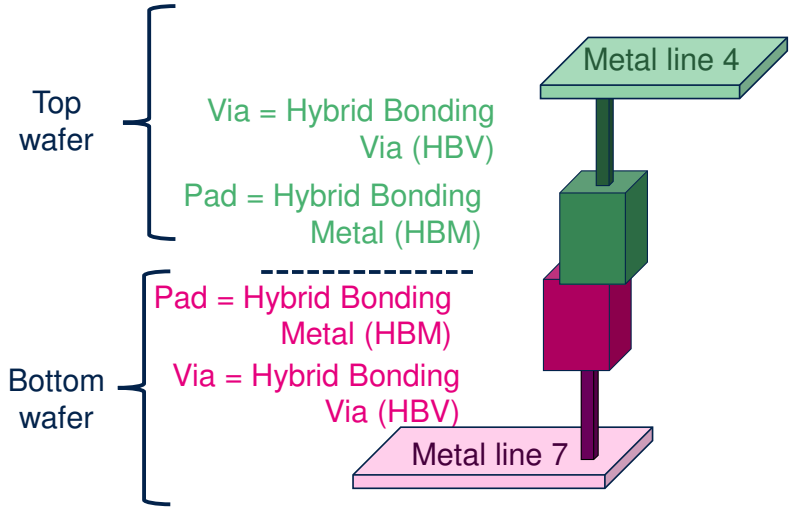
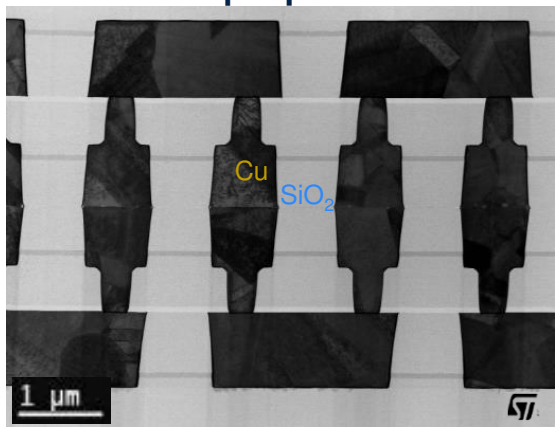
# Hybrid bonding at ST

## Double damascene integration using $Cu/SiO_2$ materials

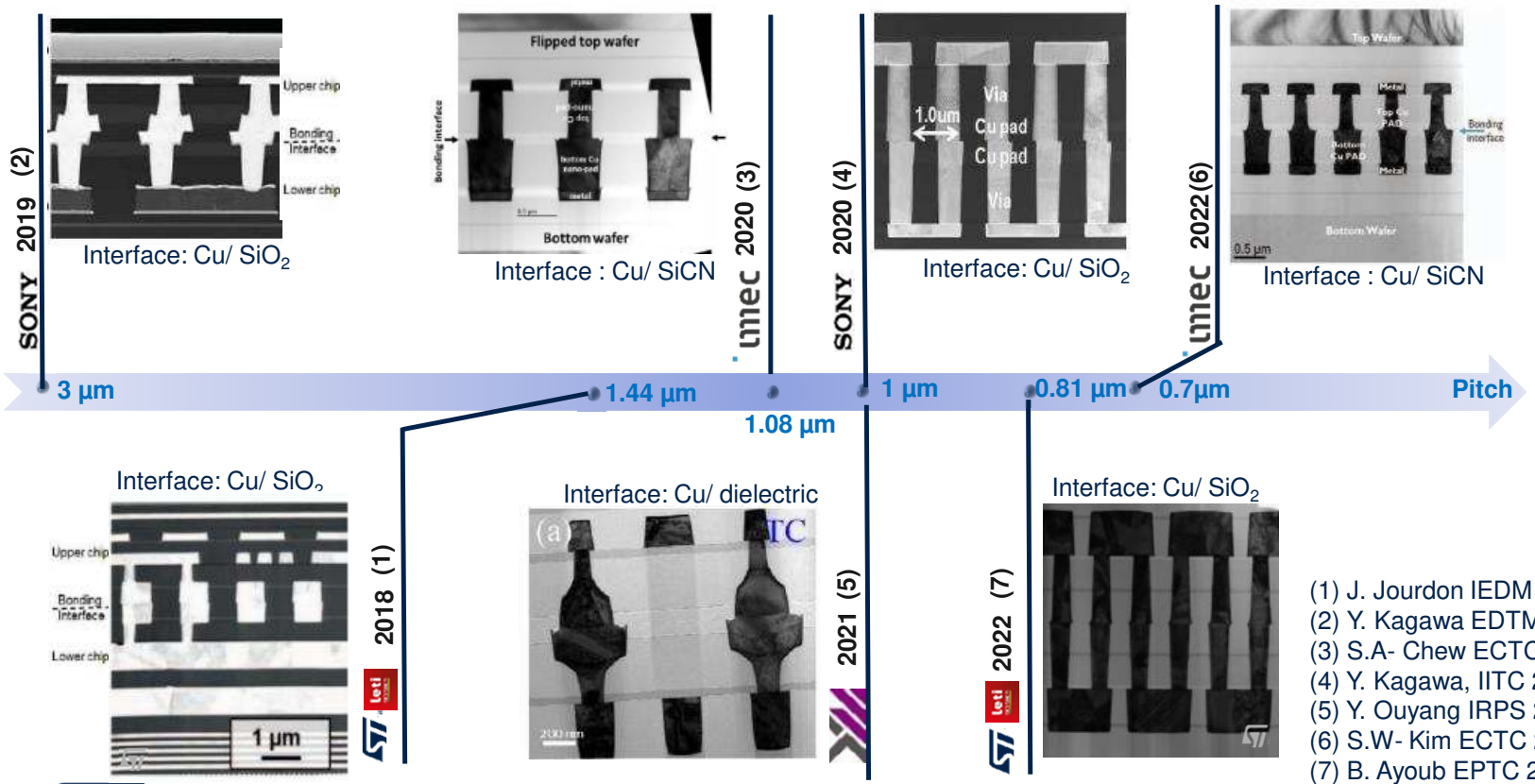



**1.44 µm pitch**



# Capability of high interconnection density

## Main demonstrations over the last 5 years




(1) J. Jourdon IEDM 2018
(2) Y. Kagawa EDTM 2019
(3) S.A- Chew ECTC 2022
(4) Y. Kagawa, IITC 2020
(5) Y. Ouyang IRPS 2021
(6) S.W- Kim ECTC 2020
(7) B. Ayoub EPTC 2022

**Challenging Sub 1µm pitch achievement**

- Using different integration at the hybrid bonding interface
- Using different configuration for pad size reduction

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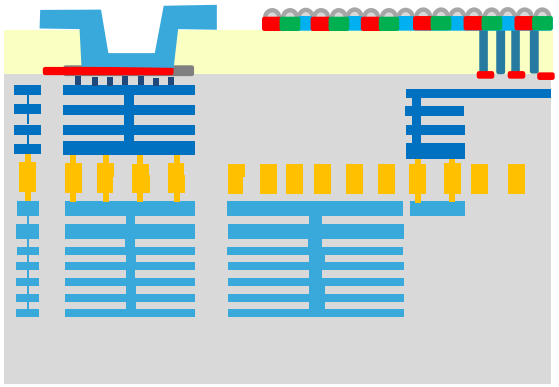
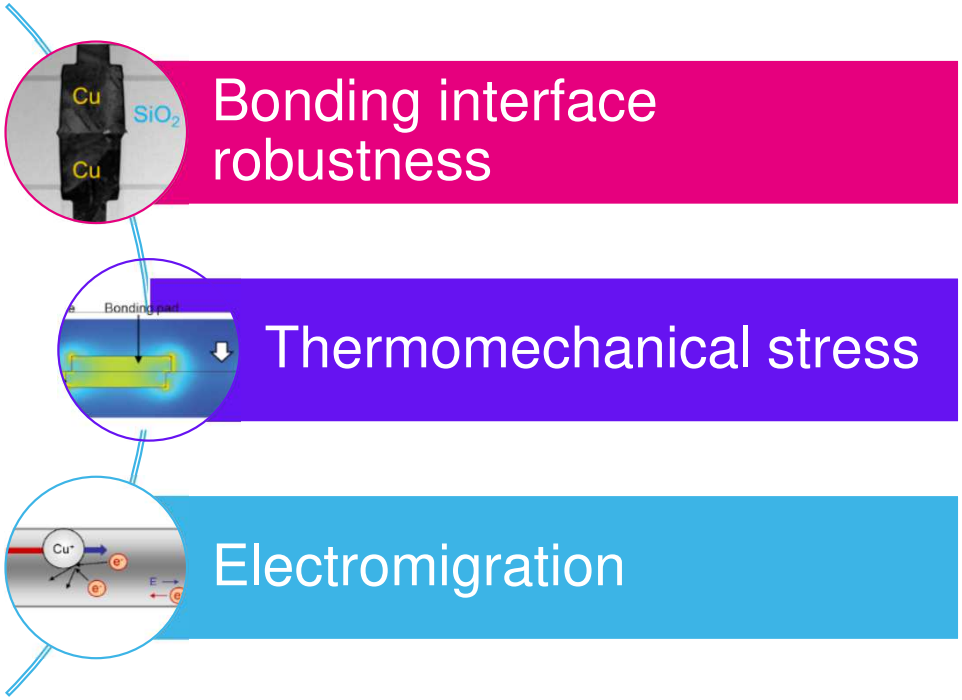
# Reliability challenges using Cu/ $SiO_2$ hybrid bonding?



**Could the hybrid bonding levels be considered as new metallization levels with specific weaknesses?**

**Is there any new concerns with pad width reduction under 1 µm?**

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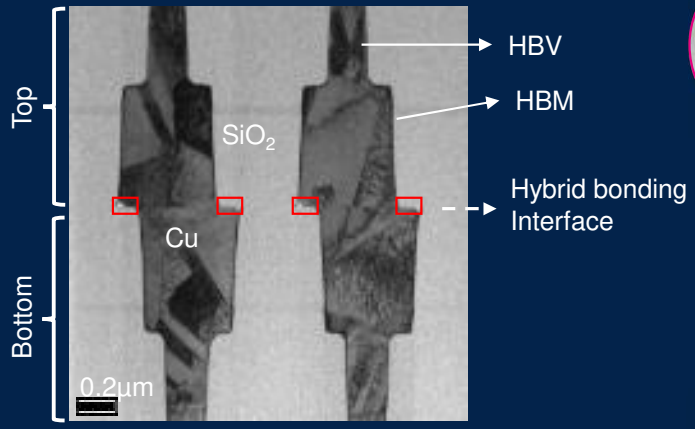
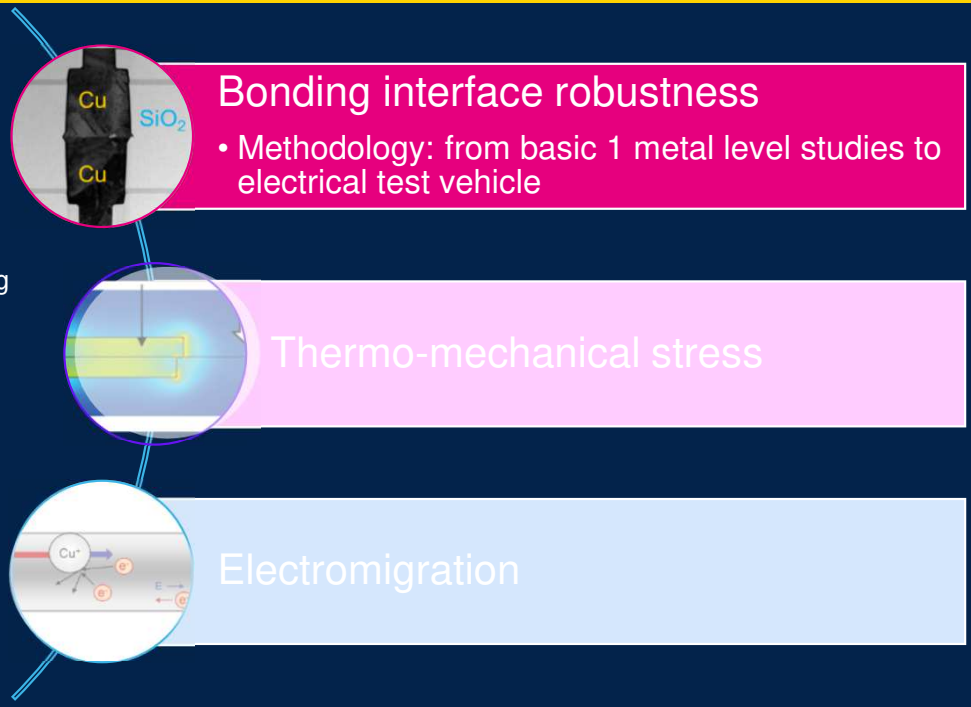
# $Cu/SiO_2$ stability at the bonding interface




**Occurrence of $Cu/SiO_2$ interfaces induced by the bonding equipment**

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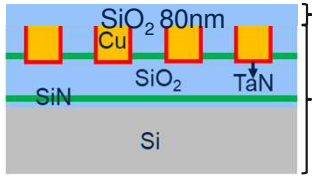
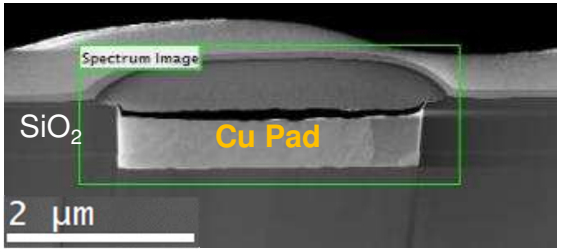
# Thermal stability of the $Cu/SiO_2$ interface

## Experiment: $SiO_2$ grown directly on Cu pads

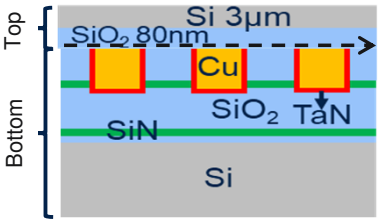



Deposited $SiO_2$
Patterned $Cu/SiO_2$




- Huge $Cu/SiO_2$ interface delamination
- Huge diffusion of Cu into $SiO_2$

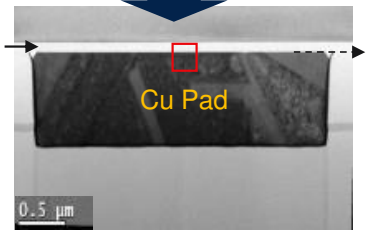
## Case of hybrid bonding $Cu/SiO_2$ (*)




Hybrid Bonding Interface

TXRF

80 nm $SiO_2$




Hybrid Bonding Interface

- Very sharp $Cu/SiO_2$ interface
- Traces of copper on the Si backside

(*) B. Ayoub et al., *Microelectronic Reliability*, **2023**, 114934

**No atomic diffusion of Cu through the hybrid bonding interface under thermal stress**

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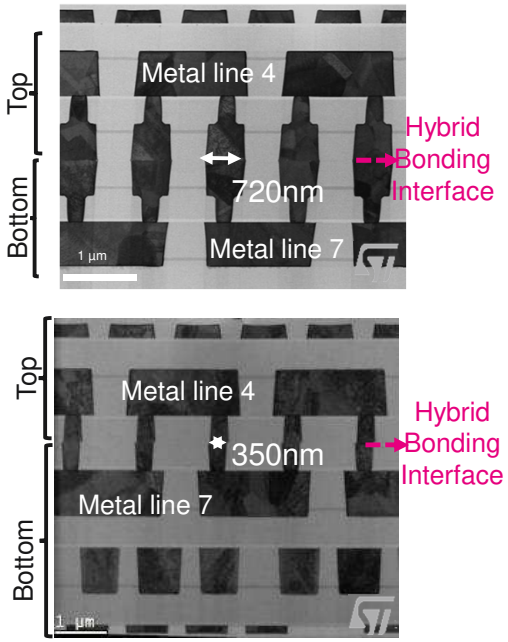
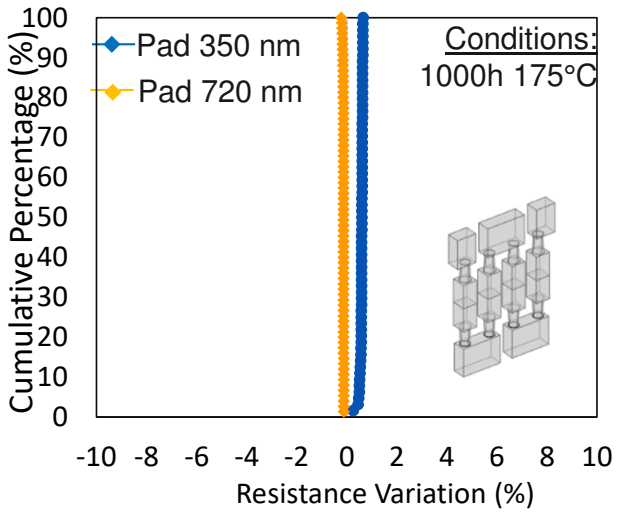
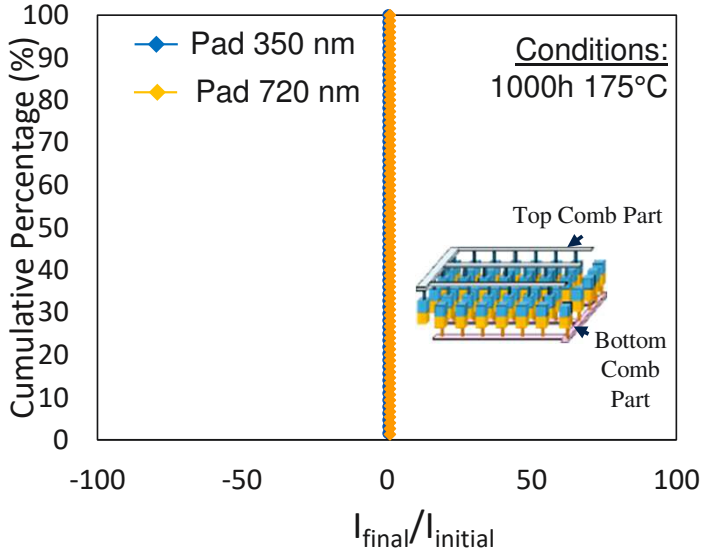
# High Temperature Storage tests

## Applied to bonding pitch 1.44µm (*)




(*) B. Ayoub et al., *IEEE 24th Electronics Packaging Technology Conference (EPTC)* **2022**, 418

**No reliability issue under thermal stress whatever the hybrid bonding pad width**

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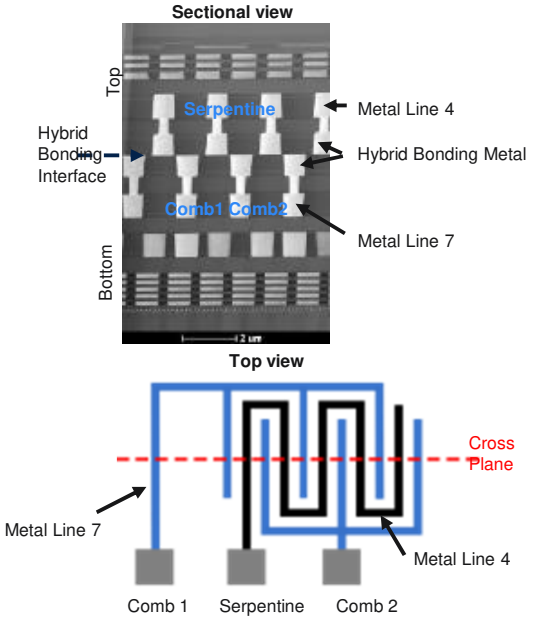
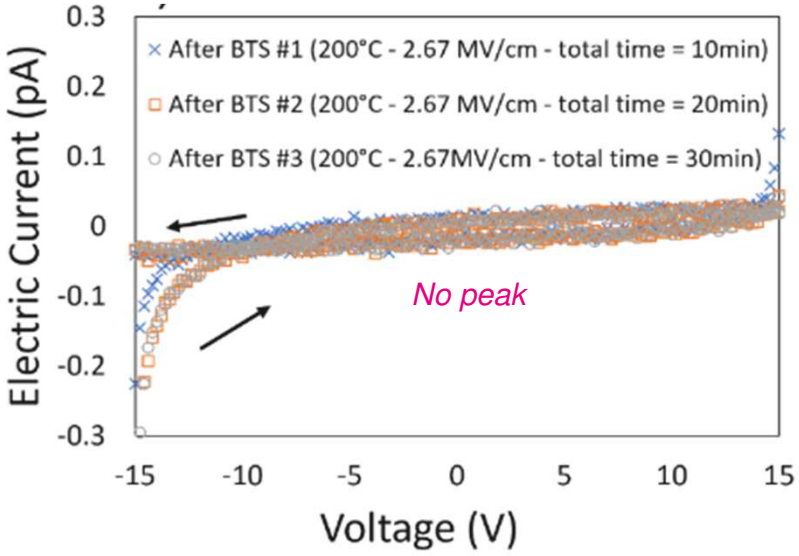
# Stability under electrical stress

## Study to detect potential ionic diffusion under electrical field

### BTS/ TVS studies on samples after HTS 4000h (*)




| | Bias Temperature Stressing | Triangular Voltage Sweep |
|---|---|---|
| **Temperature** | 200 °C | 200 °C |
| **Bias** | 2.67 MV/cm | ±15 V |
| **Duration** | Up to 30 min | - |
| **Ramp rate** | - | 125 mV/s |
| **Sweep direction** | - | -15 → +15 → -15 V |




(*) B. Ayoub et al., *Microelectronic Reliability,* **2023**, 114934

**No Cu ionic diffusion through the hybrid bonding interface**

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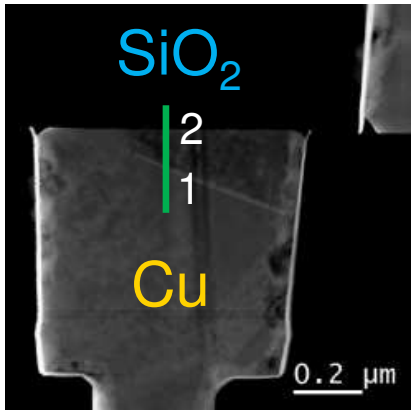
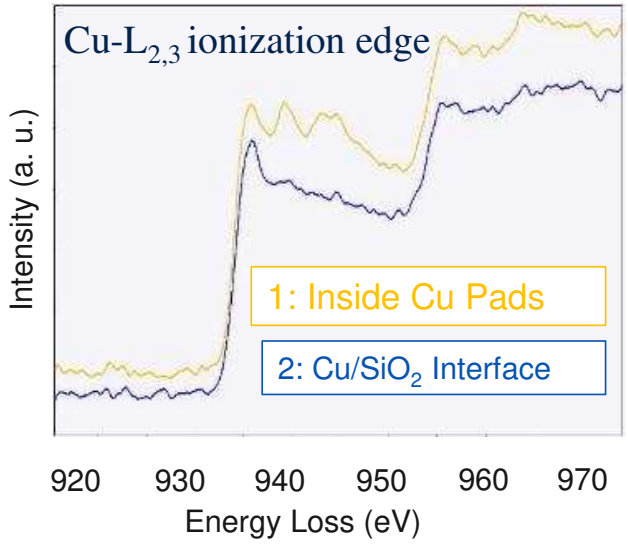
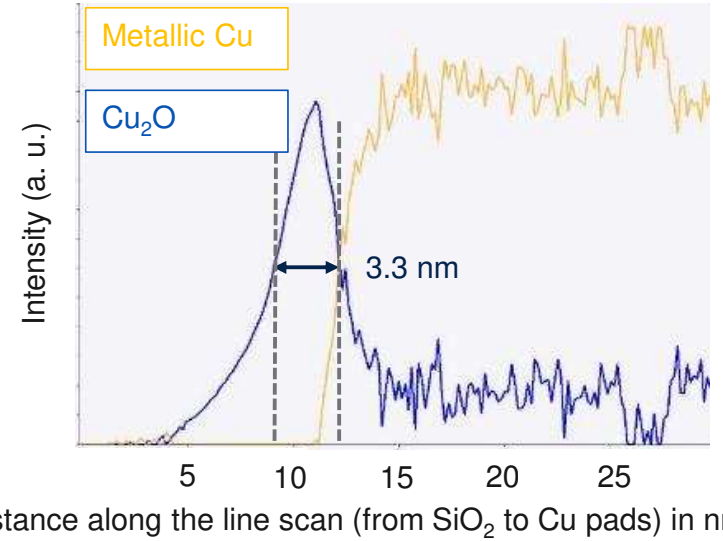
# Composition of $Cu/SiO_2$ bonding interface

**EELS analysis with probe 1 nm (*)**




(*) B. Ayoub et al., *Microelectronic Reliability,* **2023**, 114934.

**Presence of self-formed ~3nm $Cu_2O$ at the $Cu/SiO_2$ bonding interface that could act as a diffusion barrier**

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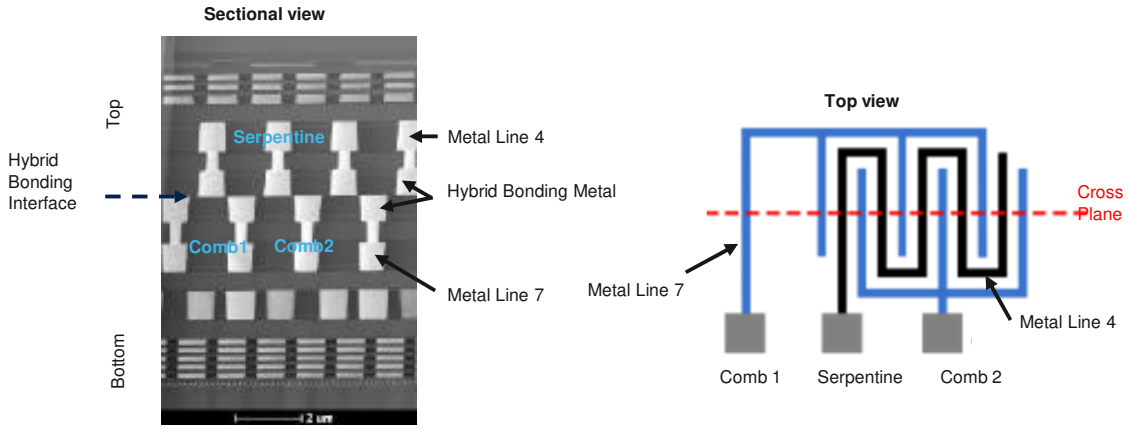
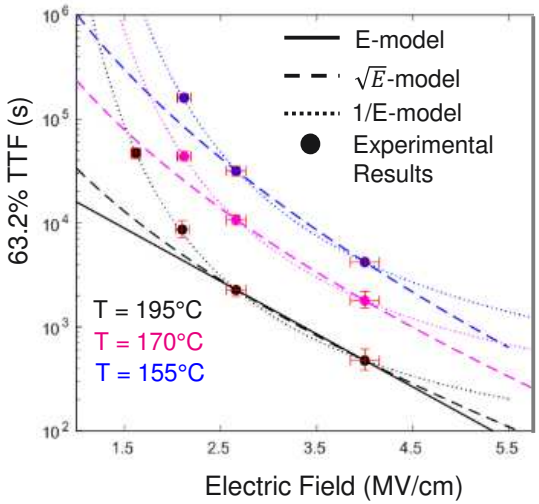
# Impact of any Cu diffusion on dielectric lifetime

## Time Dependent Dielectric Breakdown (*)




(*) B. Ayoub et al., *IEEE International Reliability Physics Symposium (IRPS)* ***2022***

- **1/E model for hybrid bonding while √ E is obtained for other BEoL levels**
- **Confirms that the role of Cu in TDDB is negligible**

**1/E dependency is attributed to the effective barrier characteristics of the Cu oxide layer**

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# Summary on hybrid bonding interface stability

No atomic or ionic Cu diffusion into $SiO_2$ under thermal stress

No reliability issue under thermal stress

TTF depency to electrical field confirming no Cu assisted breakdown

►A self-formed copper oxide diffusion barrier at the Cu/$SiO_2$ interface

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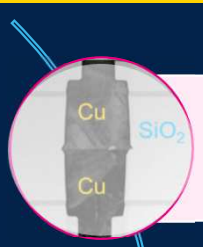
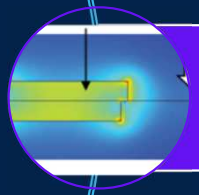
# Thermomechanical stress

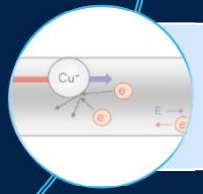



Bonding interface robustness



Thermomechanical stress

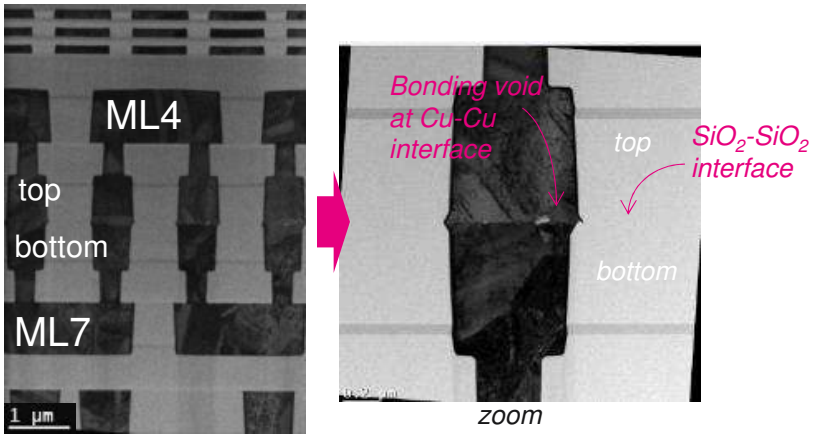
- Potential source of failures
- Thermal cycling Tests



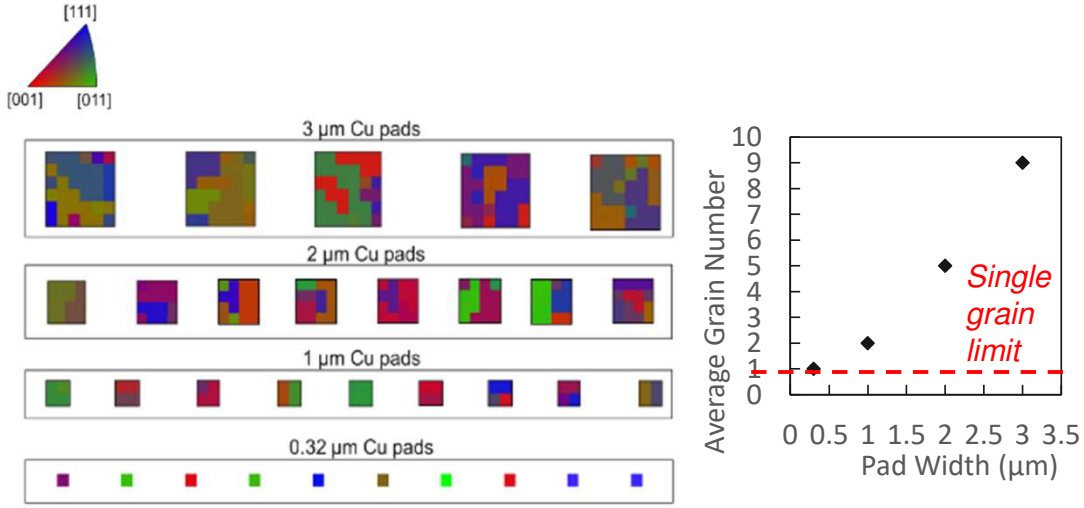

Electromigration

# Interface mechanical stability

## Cu-Cu interface reconstruction (*)




## Cu pad Microstructure by Laue microdiffraction (**)




(*) B. Ayoub et al., *IEEE 22nd Electronics Packaging Technology Conference (EPTC)* **2020**

(**) B. Ayoub et al., *Microelectronic Engineering* **2022**, *261*, 111809

**Potential interface delamination under thermomechanical stress with potential different pad reconstruction depending on the pad width**

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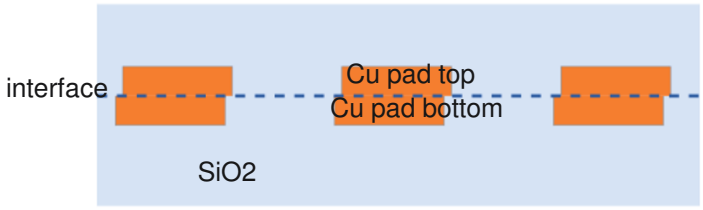
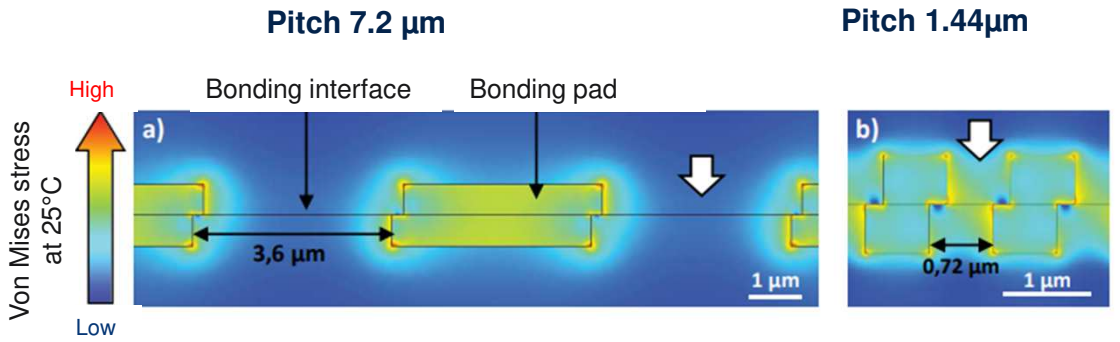
# Stress at the hybrid bonding level

## Thermomechanical simulation for the bonding pad level (*)




(*) J. Jourdon, *International Electron Devices Meeting (IEDM)* **2018**

**Stress at the hybrid bonding level is modified with pad width : potential impact on the robustness to thermomechanical stress**

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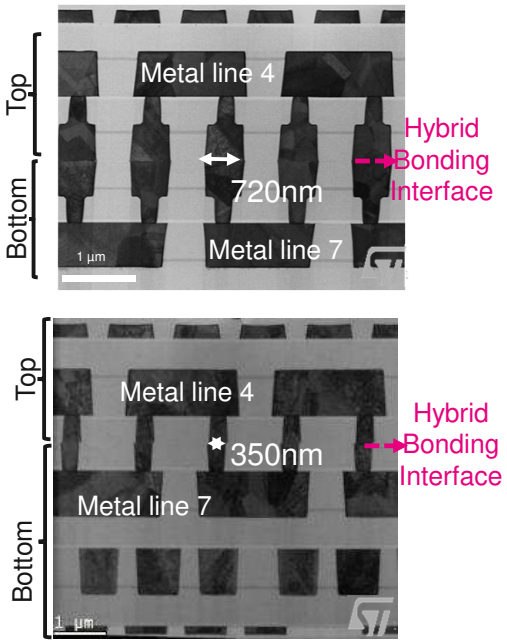
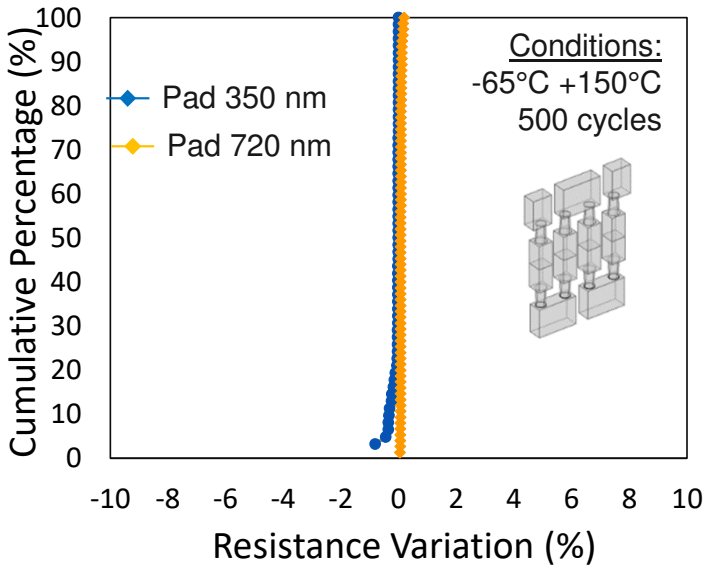
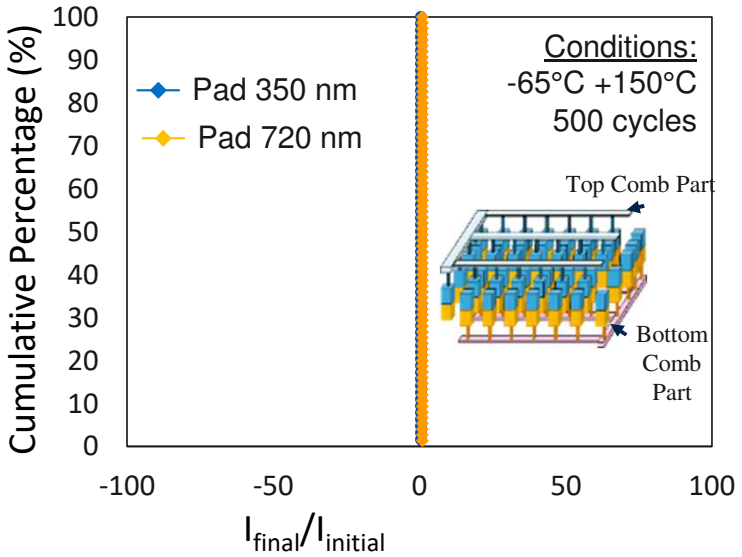
# Thermal Cycling Tests

## Applied to bonding pitch 1.44µm (*)




(*) B. Ayoub et al., *IEEE 22nd Electronics Packaging Technology Conference (EPTC)* **2020**

(*) B. Ayoub et al., IEEE 24th Electronics Packaging Technology Conference (EPTC) **2022**, 418

**No impact of hybrid bonding pad width reduction under Thermal Cycling Tests**

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# Summary on robustness to thermomechanical stress

The evolution of the Cu pad microstructure with Cu pad size could cause differences on Cu-Cu pad reconstruction

The results of the thermomechanical simulations show higher stress for smaller pitches

► However hybrid Level down to 350nm Cu pad width is reliable towards thermomechanical stress

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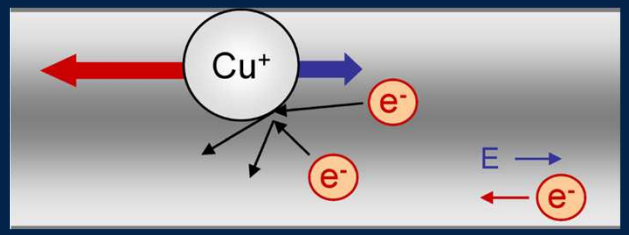
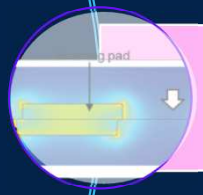
# Electromigration



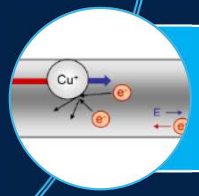

**Matter displacement activated by the application of temperature and electrical current**


Bonding interface robustness

- Methodology: from basic 1 metal level studies to electrical test vehicle



Thermomechanical stress




Electromigration

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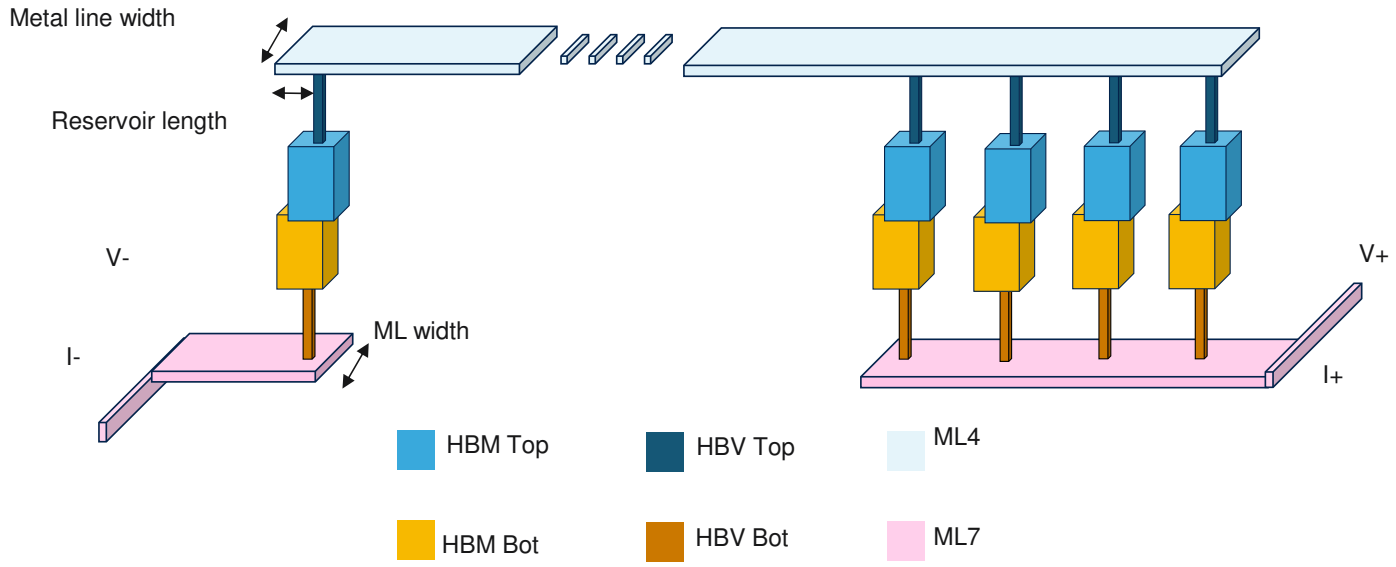
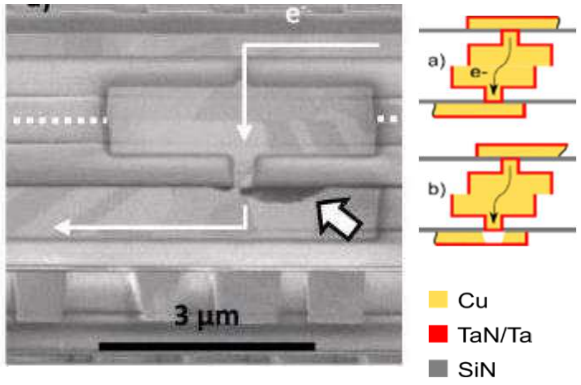
# Electromigration test structures




**NIST structures**

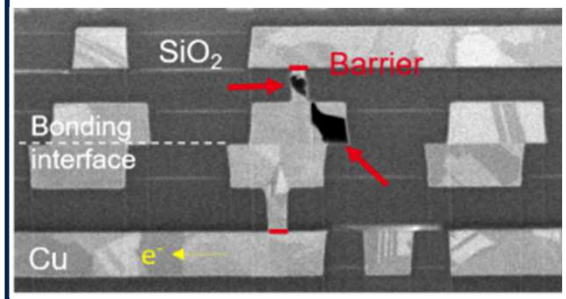
# Electromigration tests

**Pad width = 3.6 µm**

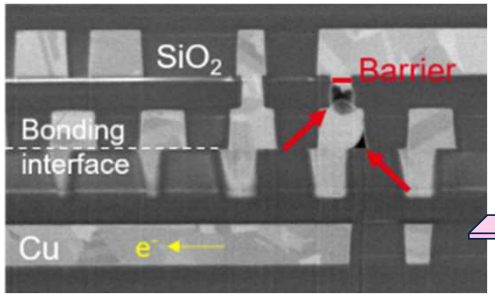


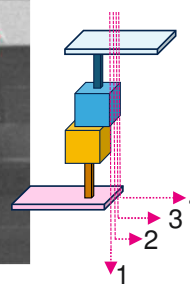

**Pad width <2 µm**

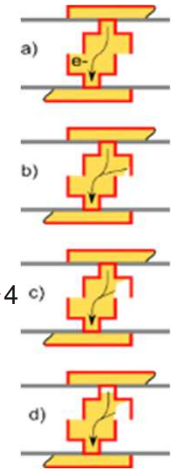
Pad width =1.7 µm




Pad width = 720nm




(*) S. Moreau et al., IEEE International Reliability Physics Symposium (IRPS) **2023**

**Lifetime is on-line with consumer specifications but identification of a modification for the failure localization with hybrid bonding pad width reduction**

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# Conclusion

# Conclusion

- **$Cu/SiO_2$ hybrid bonding level is reliable for consumer applications**
  - Robustness demonstrated as a matter of interface stability, thermomechanical stress and electromigration
- **Non-typical behavior compared to a standard back-end of line**
  - Barrier at $Cu/SiO_2$ is achieved with self formed $Cu_2O$
  - Modified TTF model with 1/E relation
  - Contribution of the hybrid bonding interface as potential failure mode under electromigration stress
- **Hybrid bonding with sub-1µm pad still leads to reliable devices**
  - No impact of pad microstructure modification
  - Lifetime is not modified by the electromigration mechanism

**Hybrid bonding stacking is mature for:**

- **Very high interconnection by pitch reduction**
- **Heterogeneous integration**

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This work has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 826600 (project VIZTA)

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