IRSP 2023

FinFETs: Sensing and Feeling Mechanical Stress

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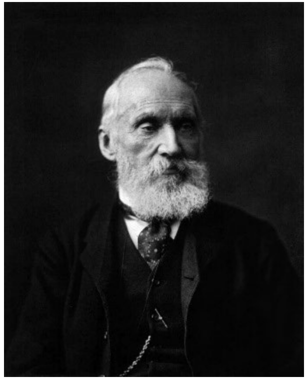
Introduction

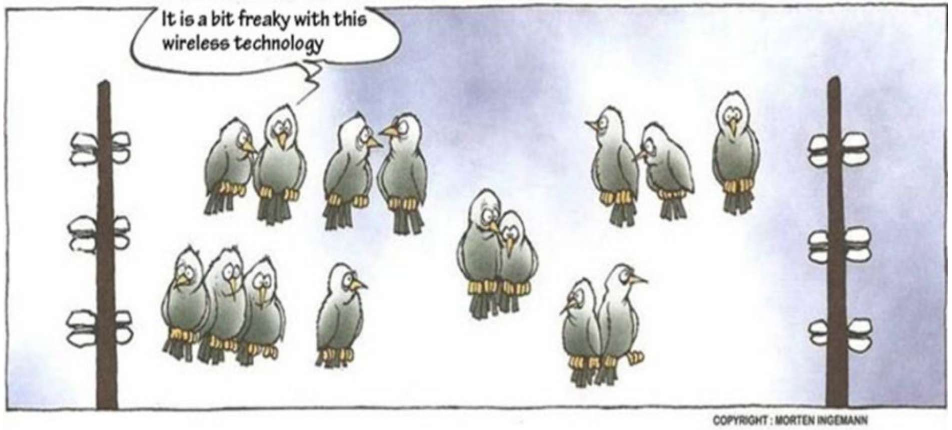
Piezoresistive effects in metals (1856 - 1935)

Lord Kelvin (1856), Cookson (1935)



1856: Lord Kelvin first reported that the resistance of iron and copper changes with elongation

Which was a problem for telegraph wire signal propagation. Studying that made him rich and famous.

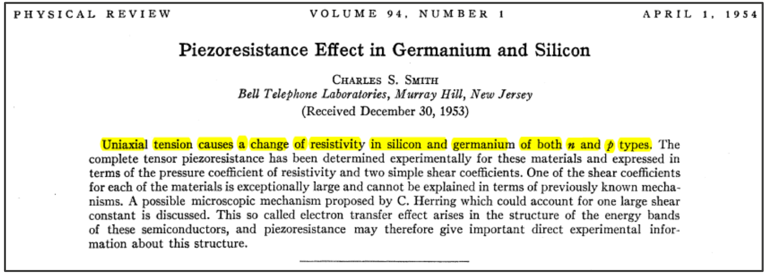


That problem is solved now...

1935: Cookson first applied the term '**piezoresistance**'

Piezoresistive effect in Si and Ge (1953)

Smith



PHYSICAL REVIEW VOLUME 94, NUMBER 1 APRIL 1, 1954

Piezoresistance Effect in Germanium and Silicon

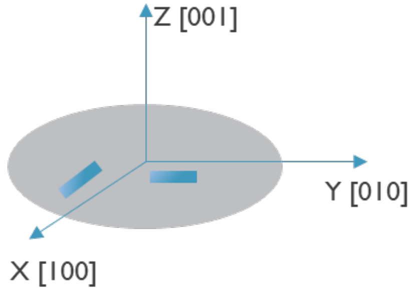
Charles S. Smith
Bell Telephone Laboratories, Murray Hill, New Jersey

(Received December 30, 1953)

Uniaxial tension causes a change of resistivity in silicon and germanium of both *n* and *p* types. The complete tensor piezoresistance has been determined experimentally for these materials and expressed in terms of the pressure coefficient of resistivity and two simple shear coefficients. One of the shear coefficients for each of the materials is exceptionally large and cannot be explained in terms of previously known mechanisms. A possible microscopic mechanism proposed by C. Herring which could account for one large shear constant is discussed. This so called electron transfer effect arises in the structure of the energy bands of these semiconductors, and piezoresistance may therefore give important direct experimental information about this structure.

- Mechanical stress affects the mobility of carriers: changes the resistivity
- The relation between resistivity, ρ, and stress, σ, in silicon and germanium (diamond lattice) is commonly described by the piezo-resistivity tensor (π_{ij})

$$\frac{1}{\rho}\begin{bmatrix}\Delta\rho_{11}\\ \Delta\rho_{22}\\ \Delta\rho_{33}\\ \Delta\rho_{12}\\ \Delta\rho_{23}\\ \Delta\rho_{13}\end{bmatrix}=\begin{bmatrix}\pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & \pi_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & \pi_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & \pi_{44}\end{bmatrix}\begin{bmatrix}\sigma_{11}\\ \sigma_{22}\\ \sigma_{33}\\ \tau_{12}\\ \tau_{23}\\ \tau_{13}\end{bmatrix}$$



- For example

$$\Delta\rho_{11}/\rho = \pi_{11}\sigma_{11} + \pi_{12}\sigma_{22} + \pi_{12}\sigma_{33}$$

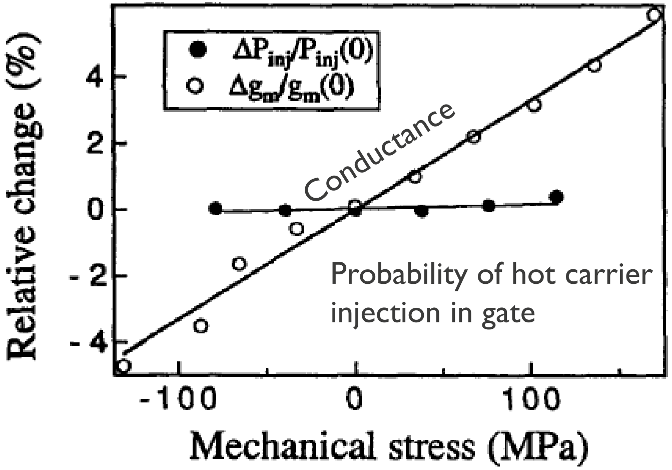
$$\Delta\rho_{22}/\rho = \pi_{12}\sigma_{11} + \pi_{11}\sigma_{22} + \pi_{12}\sigma_{33}$$

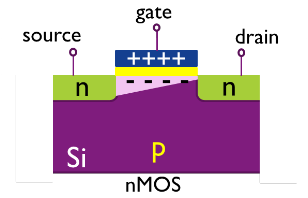
This equation was used by Smith: he measured stress induced changes in resistance.

Early experiments @ imec (1993)

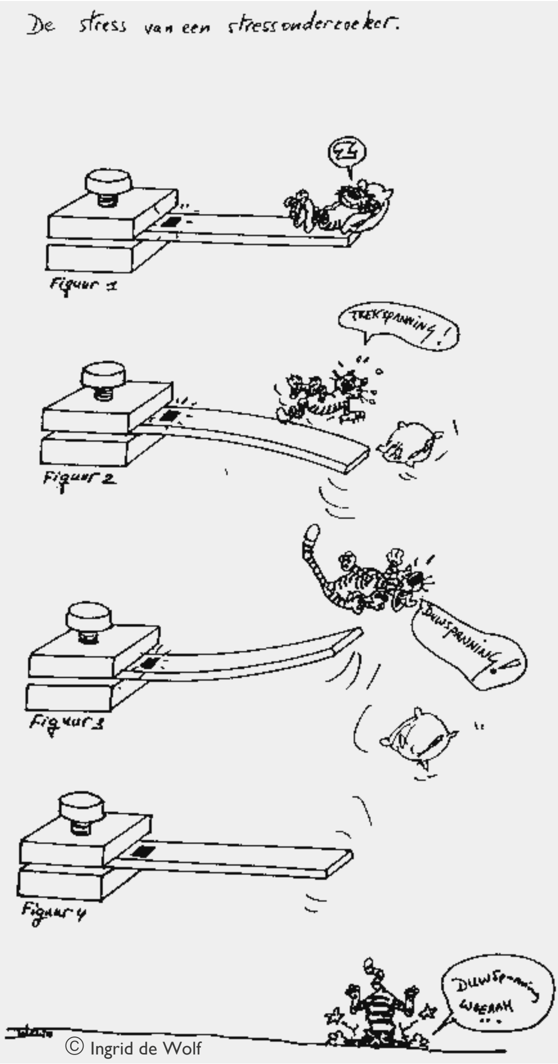
Impact of stress on gate oxide reliability

Focus on hot carrier degradation
(R. Bellens, R. Degraeve, I. De Wolf)





Instrumentation:



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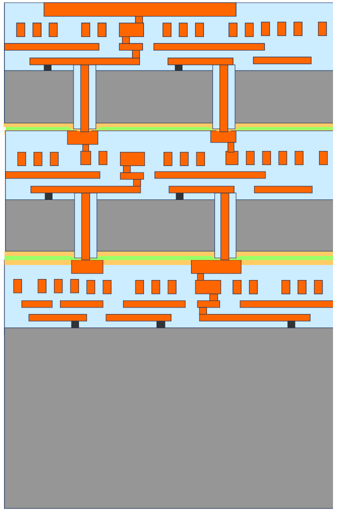
No effect on interface trap density or nr. of trapped carriers/area
(in the range +-100 MPa)
All effects are caused by mobility changes due to the **piezoresistance**

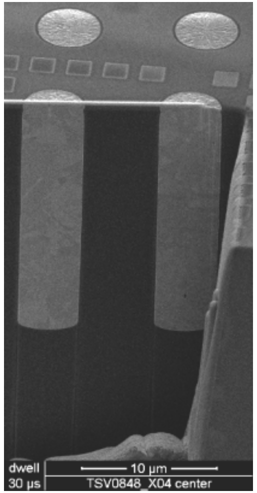
3D program at imec (2006)

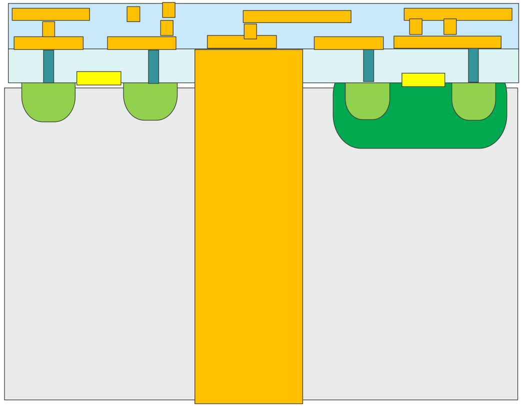
Through Si vias (TSV)

- Concern: Cu TSVs induce stress in Si
- This is expected to affect nearby transistors (piezoresistance effect).

Questions: How large is this effect? Should transistors stay a certain distance from the TSV?







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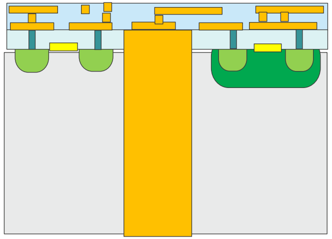
FETs feeling stress
TSV keep-out zone

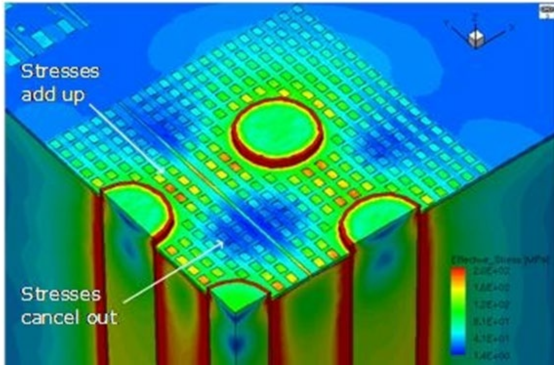
TSVs keep-out-zone

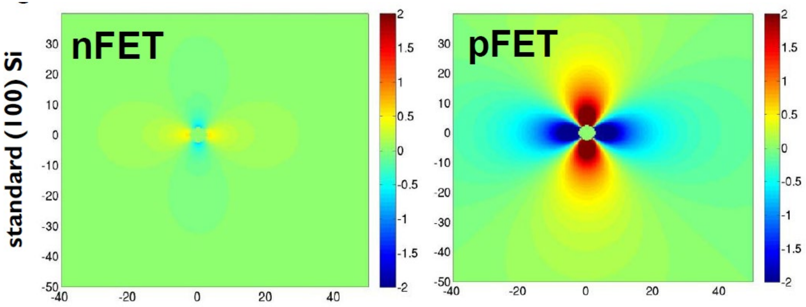
Simulations



- Simulations based on Smith data: impact stress on pFET> nFET

Based on Smith:	Electron mobility (NMOS)	Hole mobility (PMOS)
Stress parallel to channel	**+3.1% /100MPa**	**-7.2% /100MPa**
Stress perpendicular to channel	**- 1.7% /100MPa**	**+6.6% /100MPa**





Simulations

(G. Eneman)

TSVs keep-out-zone

How to measure this in a transistor? Measure I_{on}

Stress: mobility change (piezoresistance) ➡ I_{on} change

In practice, the following relation is used at imec:

$$\frac{1}{\rho}\begin{bmatrix}\Delta\rho_{11}\\ \Delta\rho_{22}\\ \Delta\rho_{33}\\ \Delta\rho_{12}\\ \Delta\rho_{23}\\ \Delta\rho_{13}\end{bmatrix}=\begin{bmatrix}\pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & \pi_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & \pi_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & \pi_{44}\end{bmatrix}\begin{bmatrix}\sigma_{11}\\ \sigma_{22}\\ \sigma_{33}\\ \tau_{12}\\ \tau_{23}\\ \tau_{13}\end{bmatrix}$$

$$\frac{1}{I}\begin{bmatrix}\Delta I_{11}\\ \Delta I_{22}\\ \Delta I_{33}\\ \Delta I_{12}\\ \Delta I_{23}\\ \Delta I_{13}\end{bmatrix}=\begin{bmatrix}\pi'_{11} & \pi'_{12} & \pi'_{12} & 0 & 0 & 0\\ \pi'_{12} & \pi'_{11} & \pi'_{12} & 0 & 0 & 0\\ \pi'_{12} & \pi'_{12} & \pi'_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & \pi'_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & \pi'_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & \pi'_{44}\end{bmatrix}\begin{bmatrix}\sigma_{11}\\ \sigma_{22}\\ \sigma_{33}\\ \tau_{12}\\ \tau_{23}\\ \tau_{13}\end{bmatrix}$$

In the [110], [-110], [001] system (devices // [110] directions)

$$\frac{1}{\rho^s}\begin{bmatrix}\Delta\rho^s{}_{11}\\ \Delta\rho^s{}_{22}\\ \Delta\rho^s{}_{33}\\ \Delta\rho^s{}_{12}\\ \Delta\rho^s{}_{23}\\ \Delta\rho^s{}_{13}\end{bmatrix}=\begin{bmatrix}\frac{1}{2}(\pi_{11}+\pi_{12})+\frac{1}{4}\pi_{44} & \frac{1}{2}(\pi_{11}+\pi_{12})-\frac{1}{4}\pi_{44} & \pi_{12} & 0 & 0 & 0\\ \frac{1}{2}(\pi_{11}+\pi_{12})-\frac{1}{4}\pi_{44} & \frac{1}{2}(\pi_{11}+\pi_{12})+\frac{1}{4}\pi_{44} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & \pi_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & \pi_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & 2(\pi_{11}-\pi_{12})\end{bmatrix}\begin{bmatrix}\sigma^s{}_{11}\\ \sigma^s{}_{22}\\ \sigma^s{}_{33}\\ \tau^s{}_{12}\\ \tau^s{}_{23}\\ \tau^s{}_{13}\end{bmatrix}$$

These coefficients are NOT the piezoresistance coefficients.

They are related to the inverse tensor (related to piezoconductivity instead of piezoresistivity)

TSVs keep-out-zone

Experiments (planar FETs at different distances from TSV)

Based on Smith:	Electron mobility (NMOS)	Hole mobility (PMOS)
Stress parallel to channel	+3.1% /100MPa	-7.2% /100MPa
Stress perpendicular to channel	- 1.7% /100MPa	+6.6% /100MPa

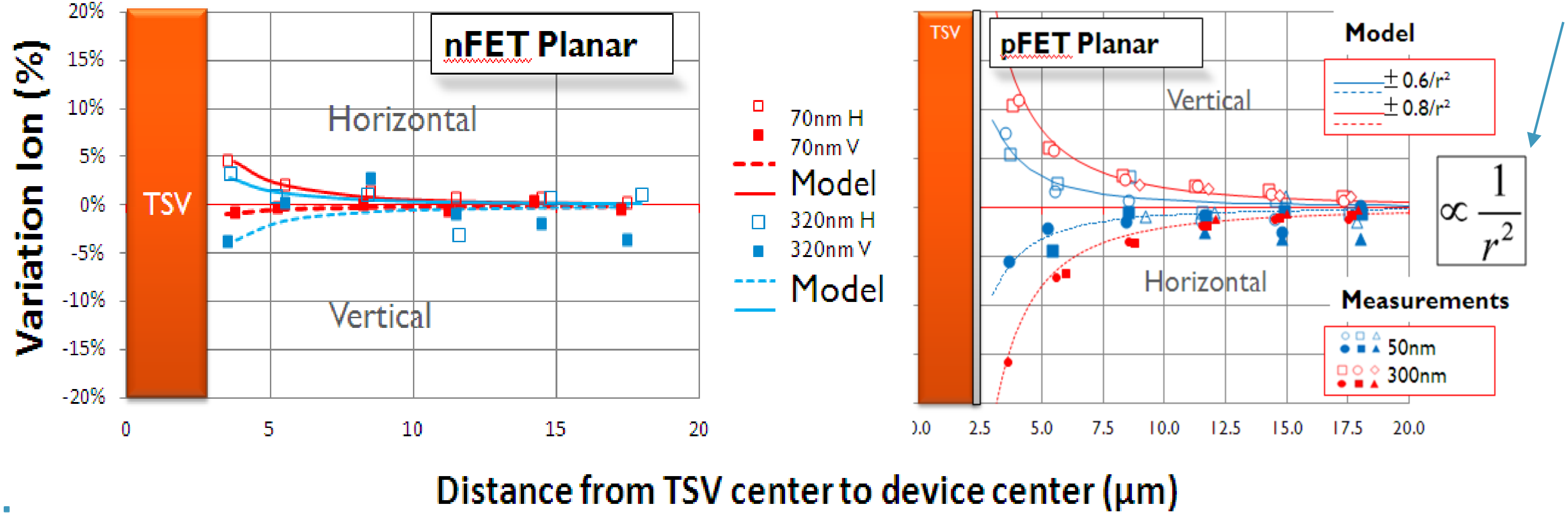
- Planar FETs are indeed stress sensitive
- PFET is more sensitive than NFET: confirms Smith data

ΔI_{on} is measured: the stress magnitude is not known: Calibration

- ☐ Lamé approximation:

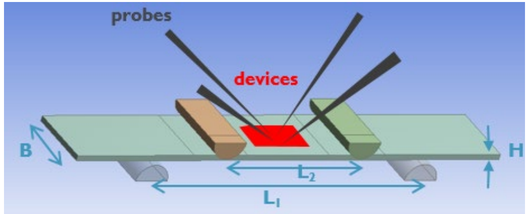
$$\sigma_r \approx -\sigma_\theta \approx -\sigma_{Cu}\left(\frac{\emptyset}{r}\right)^2$$

r = distance to TSV center

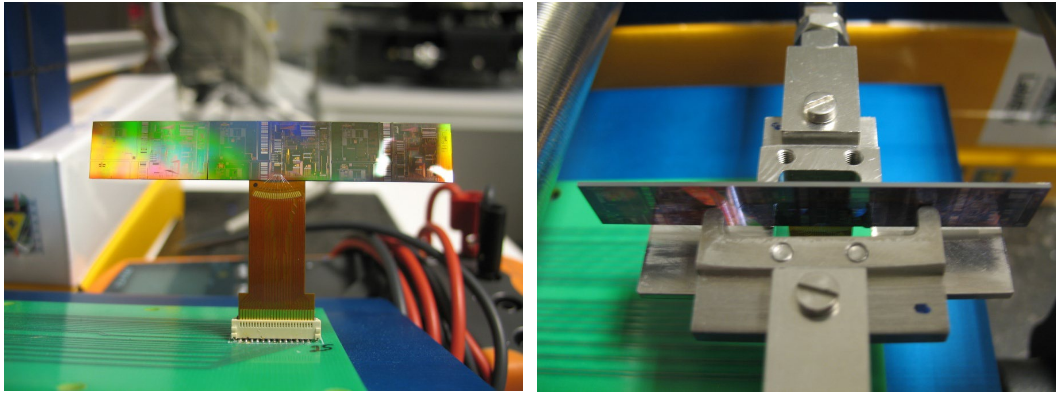


Calibration

Calibration: 4-point bending



4-point bending



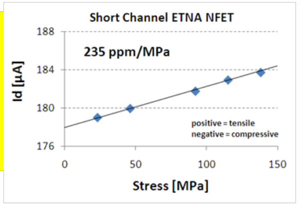
Delaminator DTS Company (Reinhold Dauskardt)

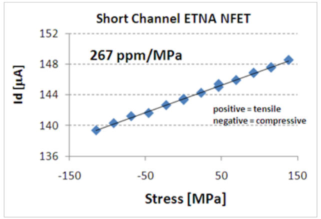
sample #1

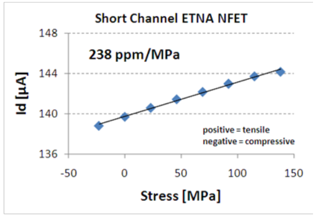
sample #4

sample #6

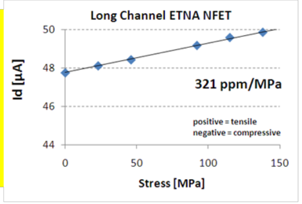
SHORT CHANNEL

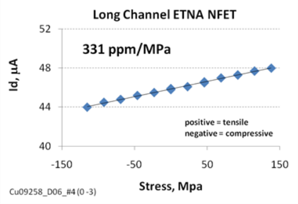


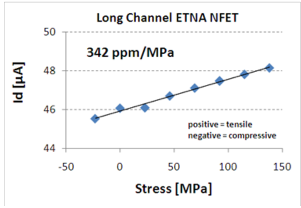




LONG CHANNEL







Applied stress ranges between -150 MPa to + 150 MPa
(risk for die cracking at higher stress)

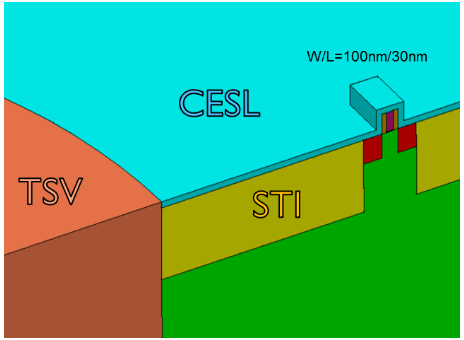
And many more experiments…

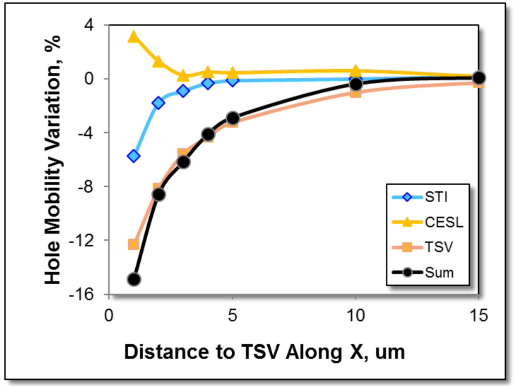
TSV-stress impact depends on technology

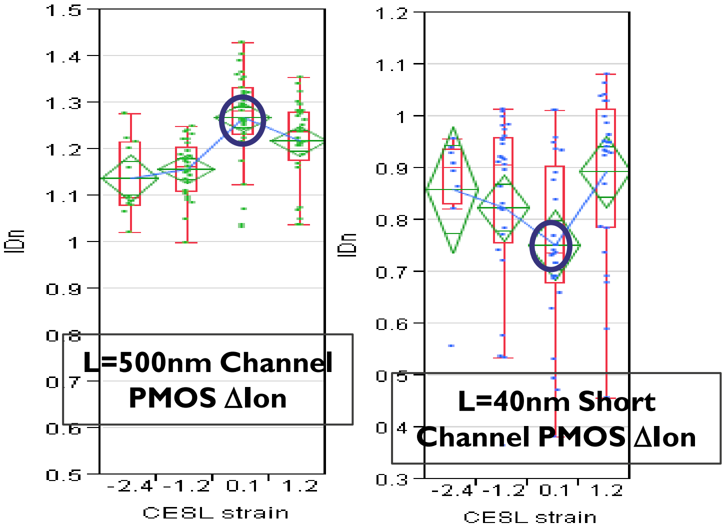
- Smidt's numbers (from 1953) are commonly used as of piezo-resistive components

BUT: results from external applied stress using 4-point bending gives different results for more modern technologies.

- Simulations and experiments indicate that TSV impact (so, stress impact) depends on strain in the channel



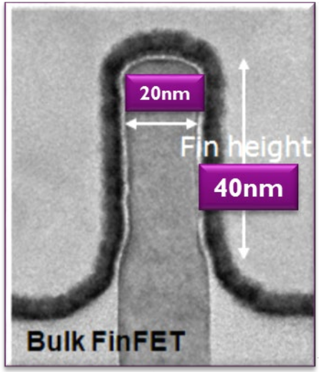



L=500nm Channel PMOS ΔIon

L=40nm Short Channel PMOS ΔIon

Planar FET versus FINFET

Using TSV induced stress

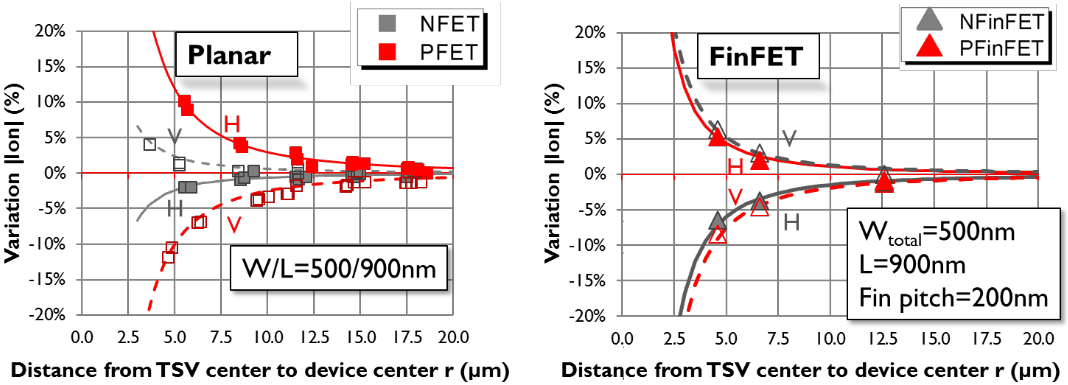


- Also FINFETS are sensitive to stress
- Planar: N type less sensitive than P type (from TSV proximity impact on Ion (at 5 μm from a TSV))
- Bulk Si FinFET: Both N and P type are sensitive (confirmed by TCAD)
- The impact of stress decreases with decreasing channel length for both planar and finFET

From TSV impact (same stress)

ΔI_{on} % @ r=5µm		Planar	FinFET
PMOS	Horizontal	-11%	-7.5%
	Vertical	11.5%	5%
NMOS	Horizontal	2.5%	5.5%
	Vertical	-2.5%	-6%

Measurements on wafers with 5x50µm TSV

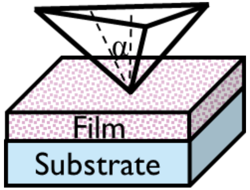


FETs feeling stress
Out-of-plane stress

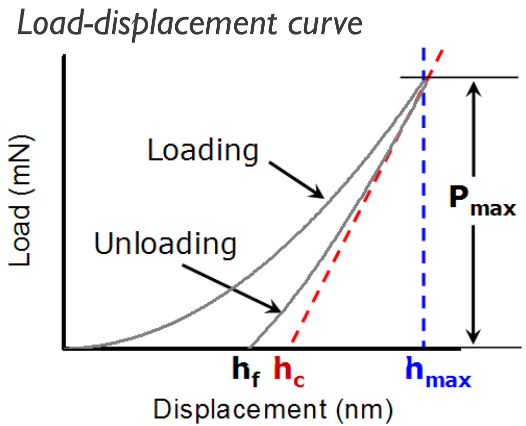
Nanoindentation

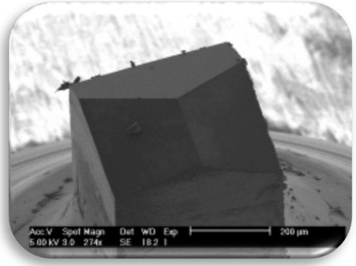
Materials focus

- Measures load-displacement curves to extract mechanical properties of films
  - Hardness
  - Elastic modulus
  - Fracture toughness
  - …
- Nanoindentation uses well defined tips (Berkovich, cube corner, spherical)



Can this be used to study impact of vertical stress on FETS?

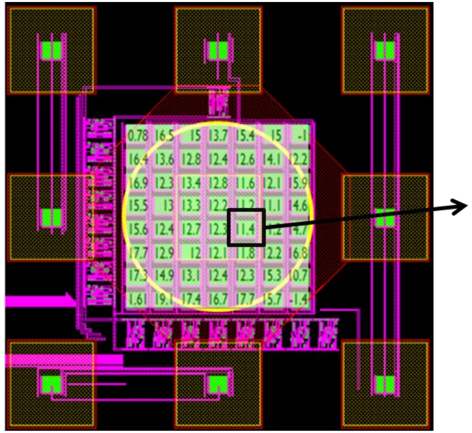




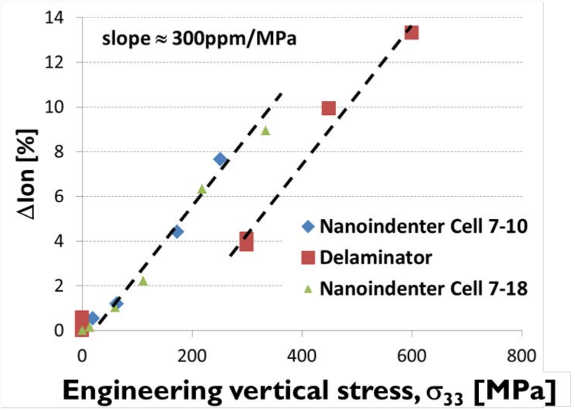
First experiments (2013)

Push on a packaged chip (need electrical access)

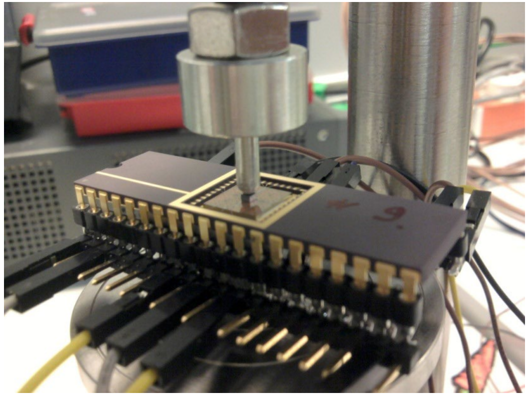
- vertical stress affects planar nFETS (PTCQ test chip)

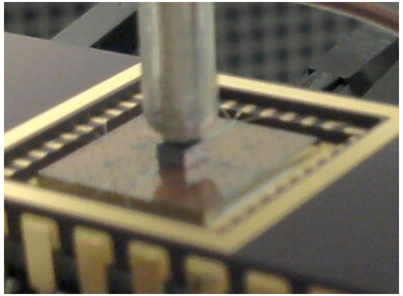


n-FET array (7x8)



/ compressive stress /

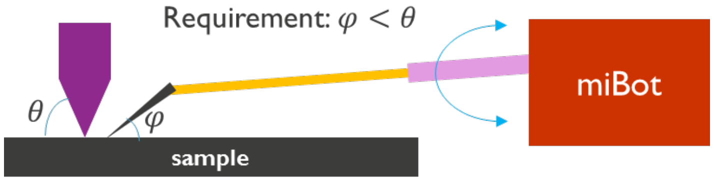




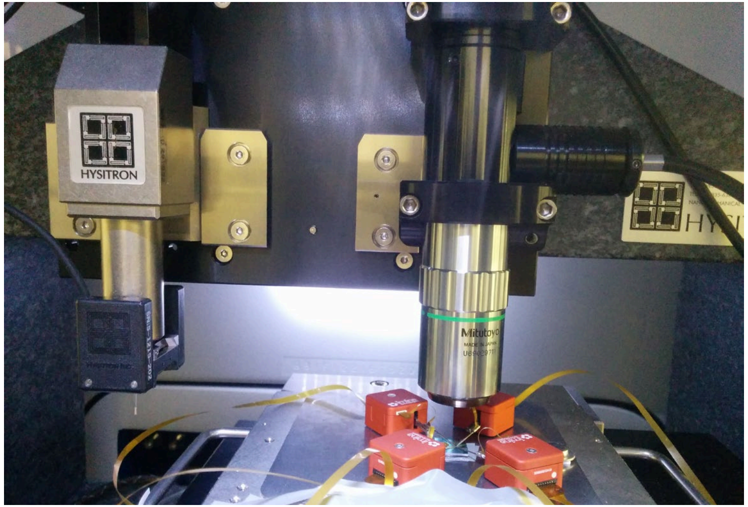
Delaminator DTS Company (Reinhold Dauskardt) (2004)

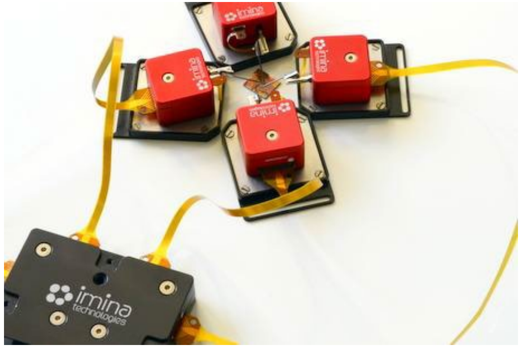
nFET' vertical gauge factor ≈ -300ppm/MPa

Nanoindentation + in-situ probing



- Use the nanoindenter (*Hysitron (Bruker)*) to apply out-of-plane stress on a device
  - Imaging mode can be used to ‘find’ the device and check the position where stress was applied
- Add small probes (miBot, *imina technologies*) for in-situ probing



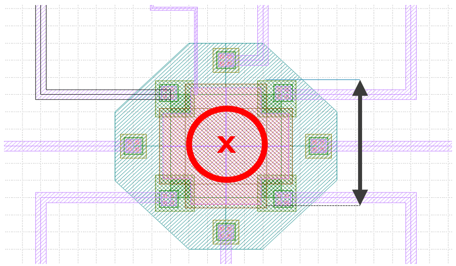


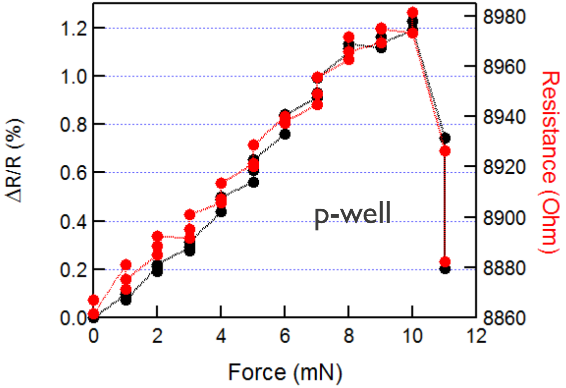
Out-of-Plane Stress impact

Resistor

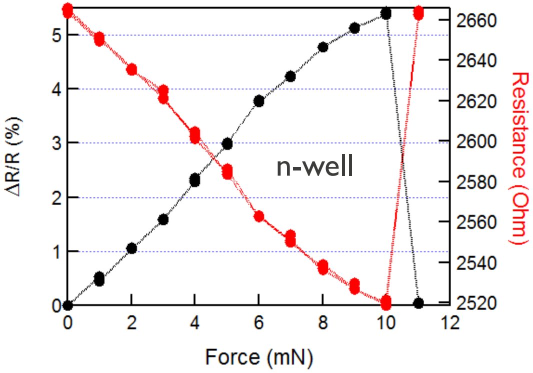
- Clear increase of the resistance with force for the p-well, and (larger) decrease for the n-well device: functionality of the set-up demonstrated

TSV+ mask (Well VanderPauw)





$$\pi_{12} = 415.3 \pm 3.4\, ppm/MPa$$



$$\pi_{12} = -24.7 \pm 0.6\, ppm/MPa$$

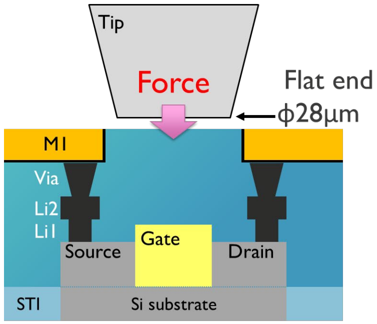
- FEM used to calculate applied stress from indentation force
- Determination of piezo-resistance coefficient (out-of-plane): good correspondence with theory (534 and -11 respectively)

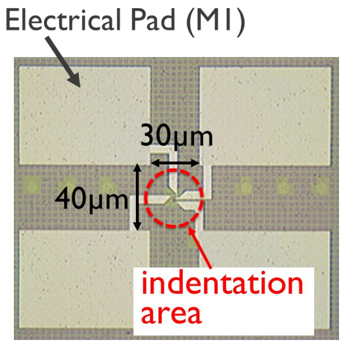
Out-of-Plane Stress impact

FINFETS (28 nm node)

Clear impact of out-of-plane force

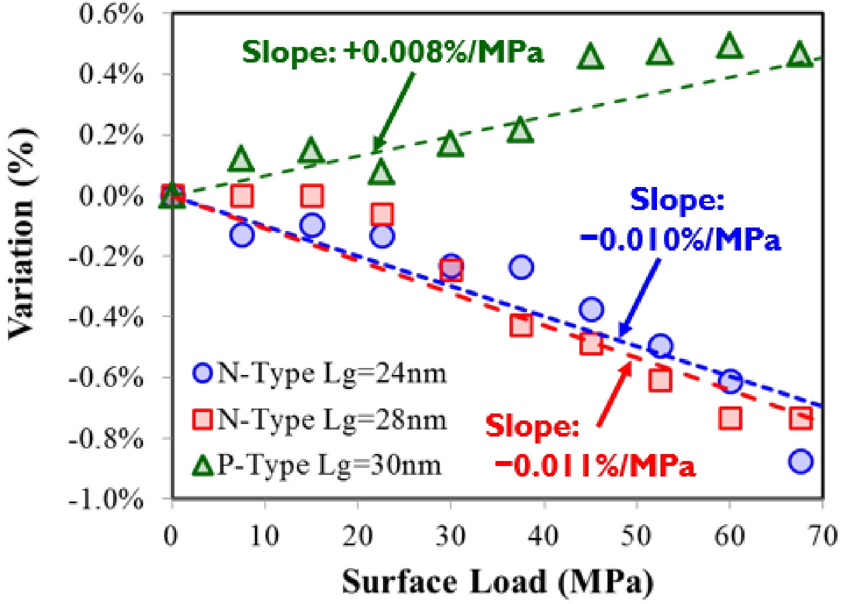
- I_d of N-Type decreases with increasing force
- I_d of P-Type increases with increasing force
- Sensitivity decreases with decreasing gate length





Surface picture

T. Furuhashi (Sony), Y. Liu, G. Hiblot

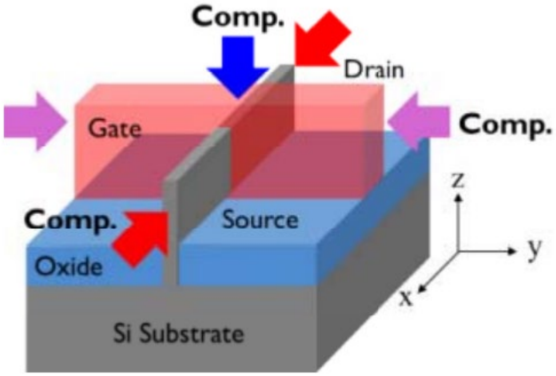


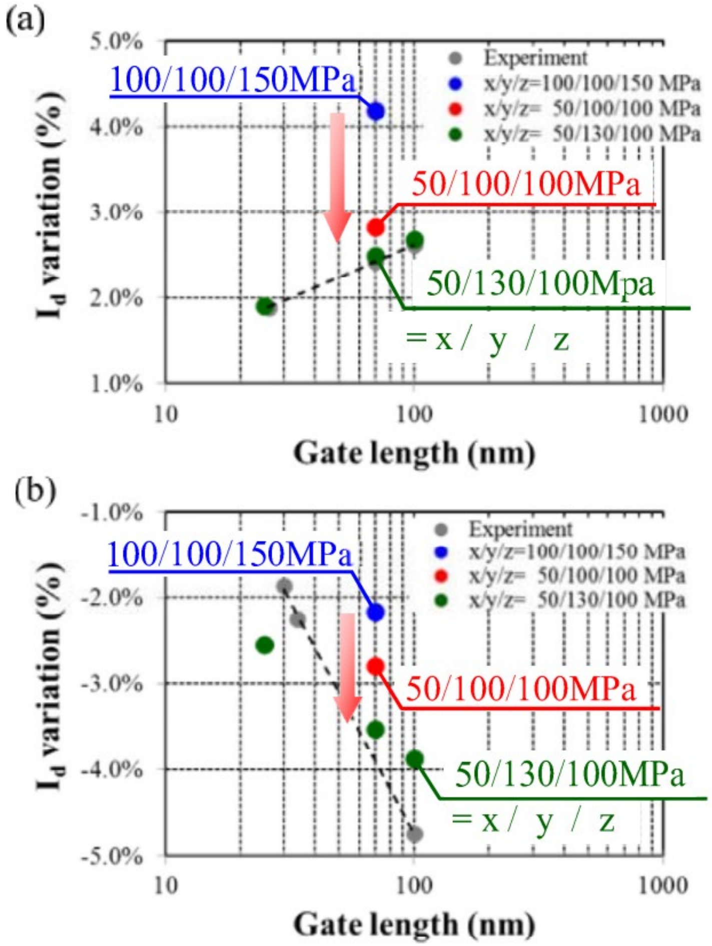
T. Furuhashi (Sony), Y. Liu, G. Hiblot

Out-of-Plane Stress impact

FINFETS (28 nm node)

BUT: Vertical force also induces in-plane compressive stress (FEM simulations). For a vertical force (z) of 200 mN: Larger stress ⊥ FIN (y) than // FIN (x) (due to stiffer gate material)



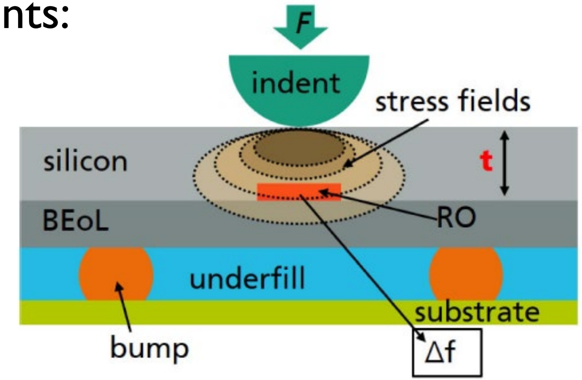


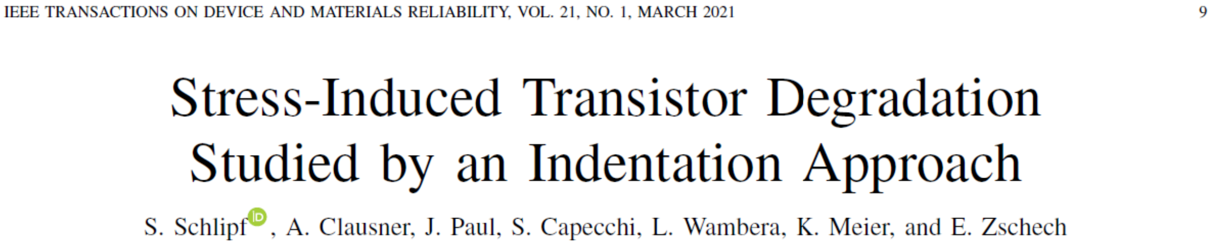
Alternative method

S. Schlipf PhD Thesis, TU Dresden, 2021

- How to distinguish impact of different stress components:

See talk Andre Clausner



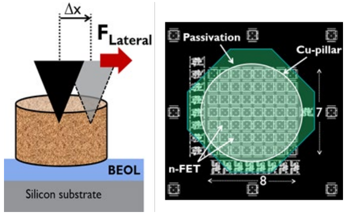

IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, VOL. 21, NO. 1, MARCH 2021 9

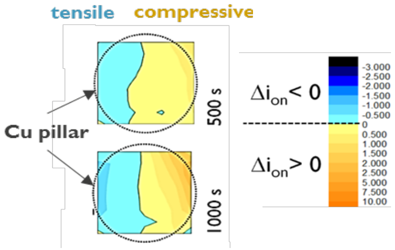
Stress-Induced Transistor Degradation Studied by an Indentation Approach

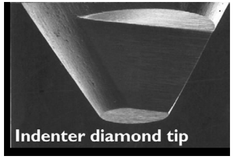
S. Schlipf, A. Clausner, J. Paul, S. Capecchi, L. Wambera, K. Meier, and E. Zschech

Impact of stress on...

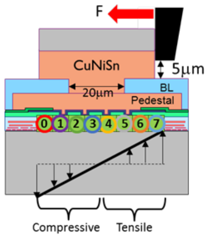
Using Hysitron/Mibot combination

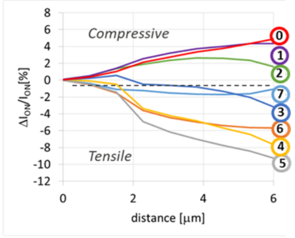


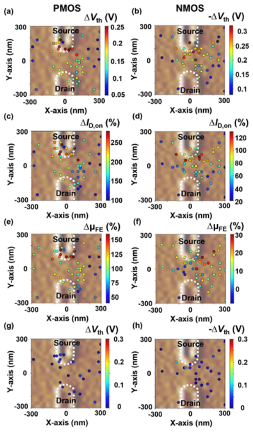




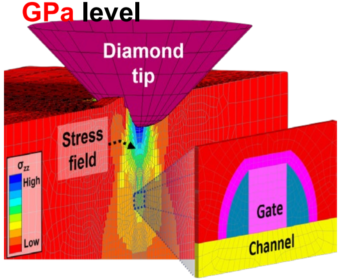
- BAPSI test/shear stress: Kris Vanstreels
- 3D memory devices: Anastasiia Kruv (PhD)
- FINFETS: Takahisa Furuhashi (Sony)
- HBT, BJT, bandgap reference circuit: Yefan Liu, Gaspard Hiblot
- Silicide contact resistivity: Yefan Liu, Gaspard Hiblot
- MOSFET local: Kookjin Lee (post doc)
- Reliability ...



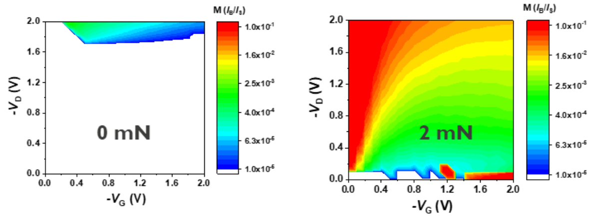


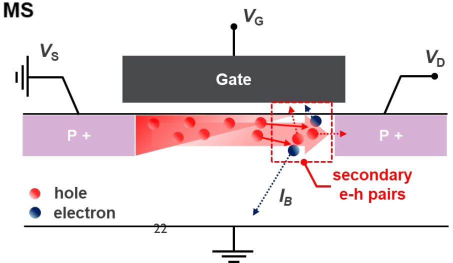


Locally induced MS up to GPa level



Strong increase in secondary-carrier (e-) generation in pFET due to MS



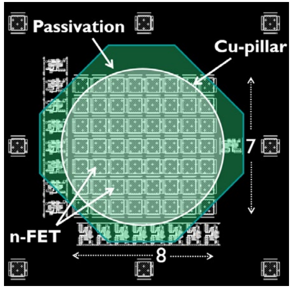


FETS sensing stress
CPI

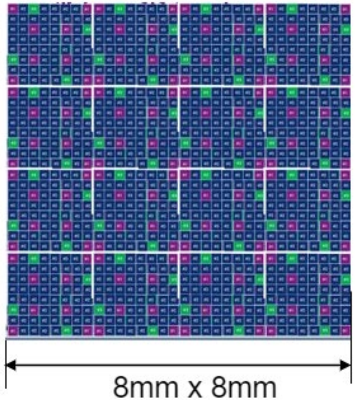
Test structures

- FETS are sensitive to stress: Can be used as stress sensor
- Various test-chips were developed at imec over the years, containing local and global ‘stress’ sensors

n-FET array (7x8)



Test chip



32 x 32 modules

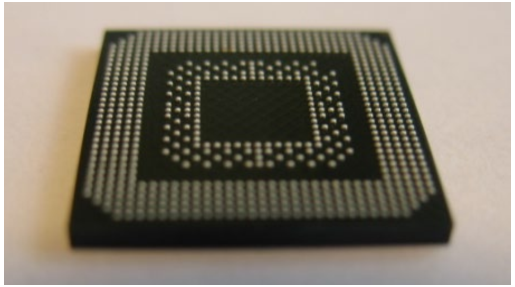
Module: 0.25mm x 0.25mm

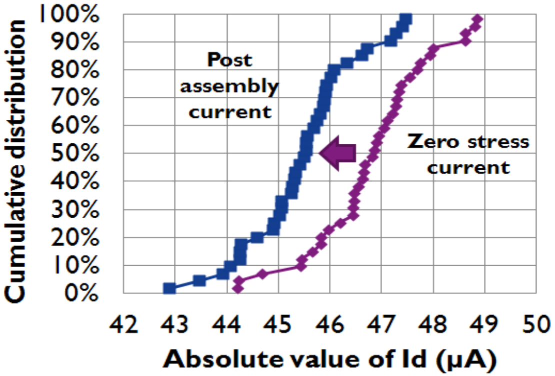
- 🟦 general CPI & Thermal
- 🟩 local stress sensors
- 🟪 BEOL stress sensors

Stress sensors:

- nFETs
- pFETs

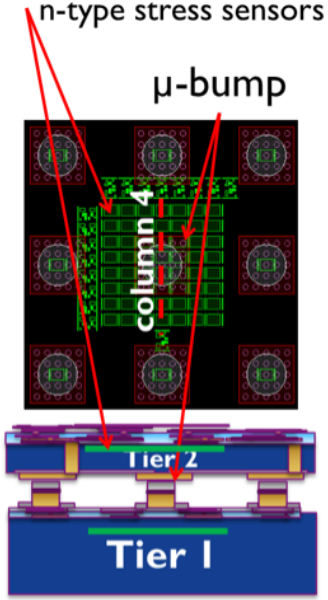
Negative current shift indicating compressive stress from shrinking overmold



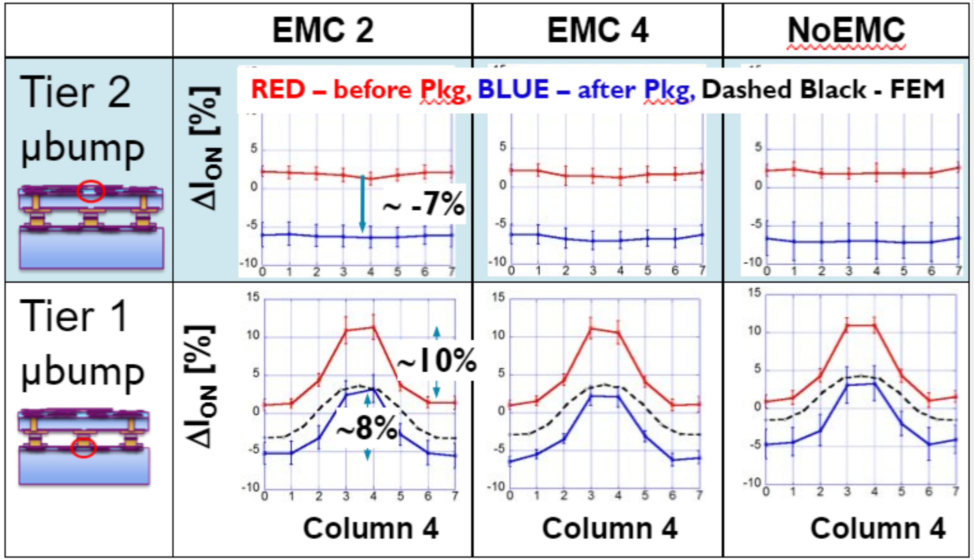


Stress around μ-bump (sensor array)

Cherman ECTC 2015



Impact overmould



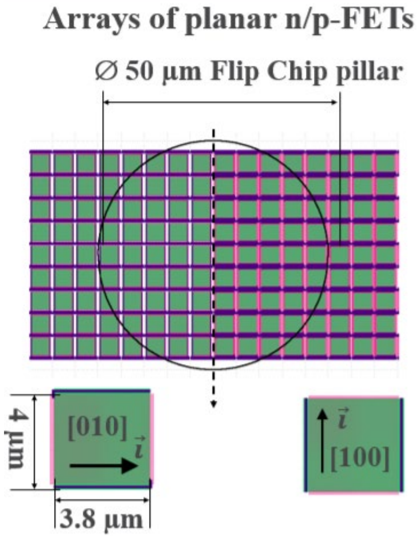
Packaging has a large effect on I_{ON}

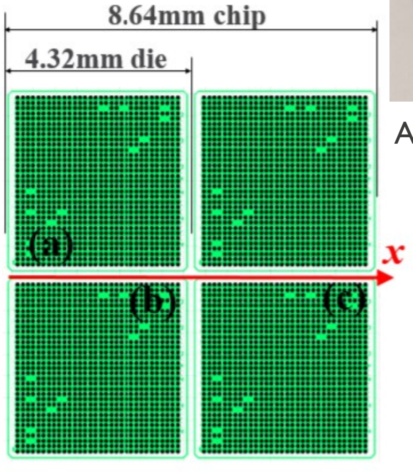
Local shape at μ-bump is preserved.

Global and local stress in flip-chip BGA package

Cherman EMPC2019

Stress test chip

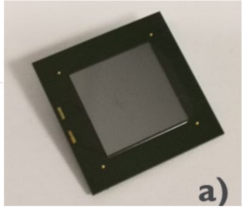




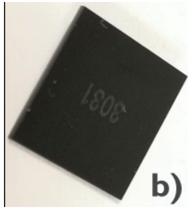
(a), (b) and (c) – locations of studied local stress

	π_{11} [ppm/MPa]	π_{12} [ppm/MPa]	π_{13} [ppm/MPa]
n-FET	300	180	-560
p-FET	-60	-210	263

calibrated equivalent piezo resistance coef.

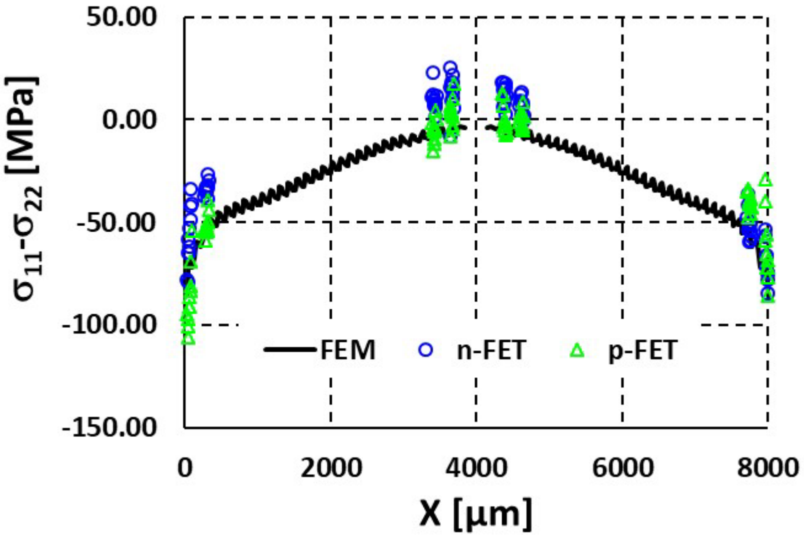


Assembled bare die



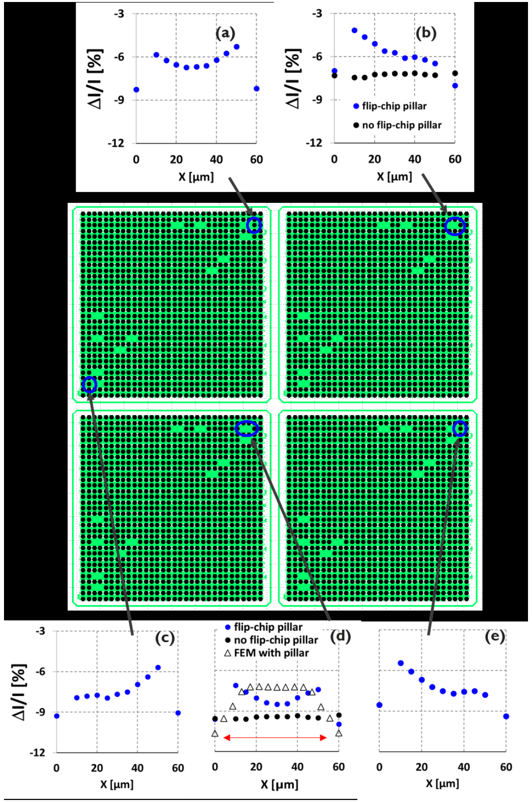
With overmould

$$\sigma_{11} - \sigma_{22} = \frac{\Delta I_0 - \Delta I_{90}}{\pi_{11} - \pi_{12}}$$

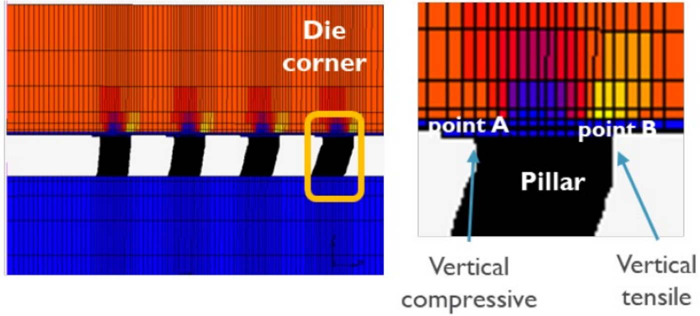


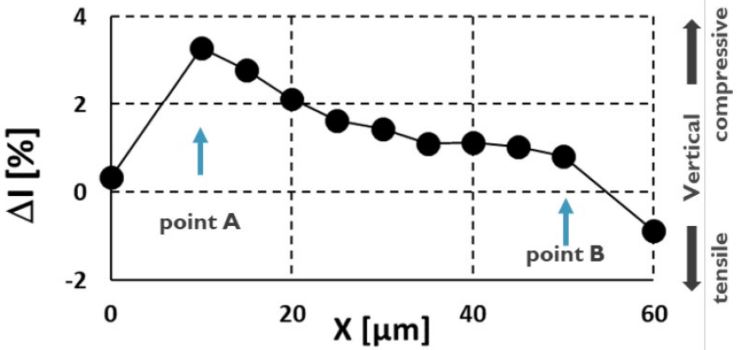
Global and local stress in flip-chip BGA package

Cherman EMPC2019



Electrical response of n-type stress sensors at different locations on the packaged test chip.

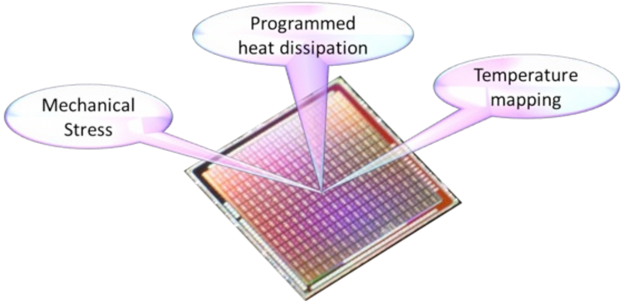


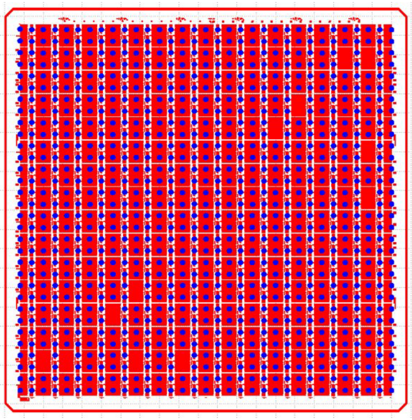


Response above pillars at the corner of the packaged die

Test chip

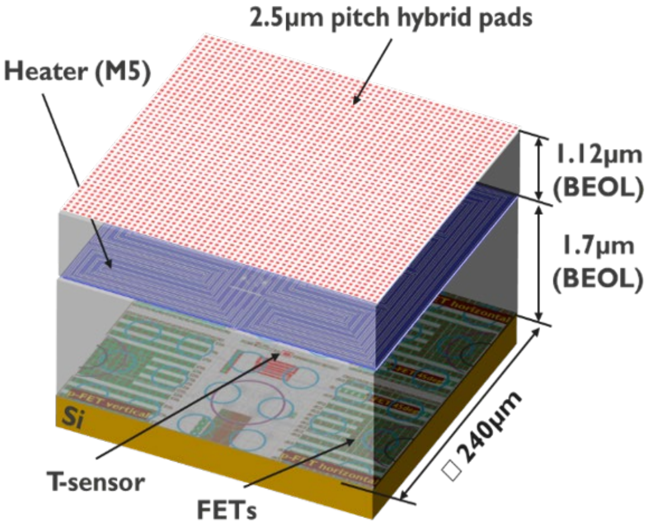
Test Chip consisting of 4.32 X 4.32 mm^2 squares contains 256 unit cells 240x240µm^2





Every unit cell contains

- temperature sensor
- programmable heater
- stress sensors
  - 744 FEOL (FETs)
  - 2 BEOL (capacitive)

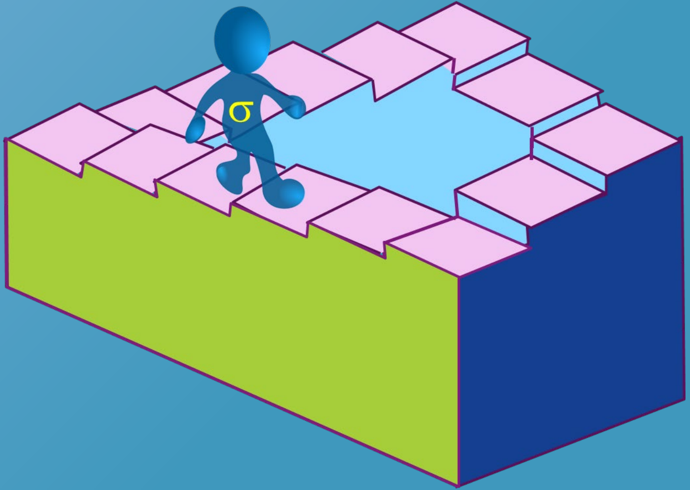


Chips are compatible with:

- Variable chip size: 4x4 mm^2 – 30x20 mm^2
- Flip-Chip, wire-bond and fan-out packaging options
- Different 3D integration schemes (3DSIC, 3DSOC, 3D interposer) including N>2

Conclusions

Stress: A never ending story in microelectronics.



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