Degradation mechanisms of 10kV-reinforced isolated gate drivers at high switching frequencies greater than 30kHz

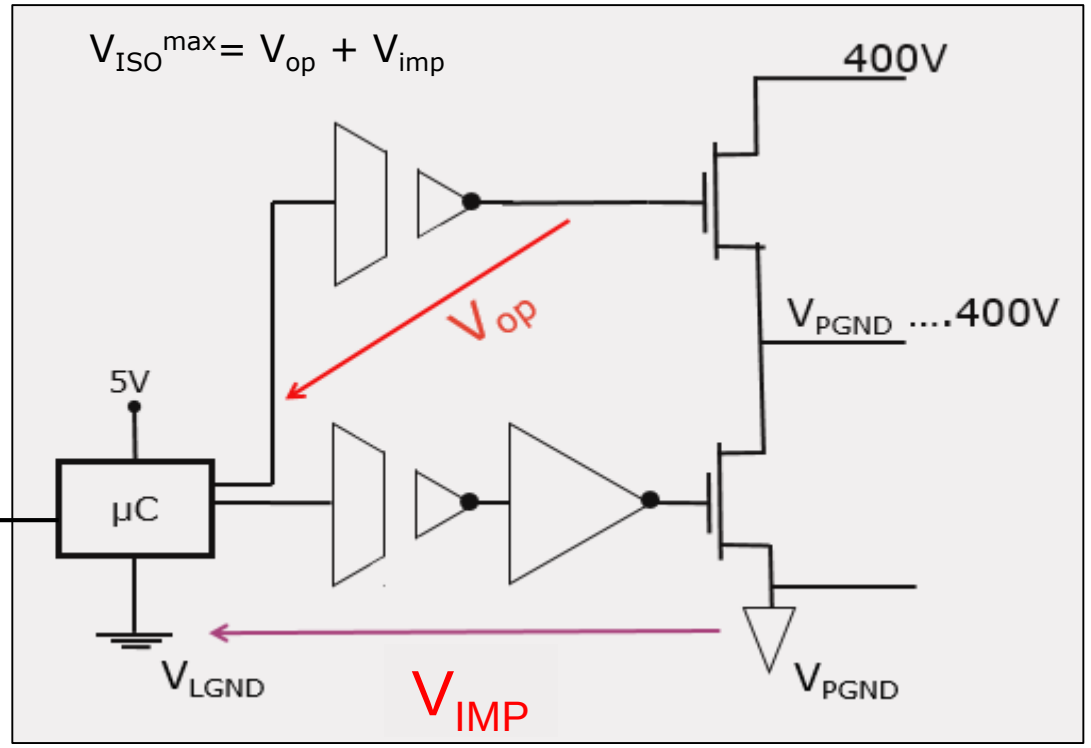
Matthias Stecher[1)], Leonard A. Dissado[2)]

[1)] *Infineon Technologies, 85579 Neubiberg, Germany; Matthias.Stecher@infineon.com*
[2)] *Prof. Emeritus, Dep. of Eng., Uni. of Leicester, Uni. Road, Leicester, LE1 7RH, U.K*

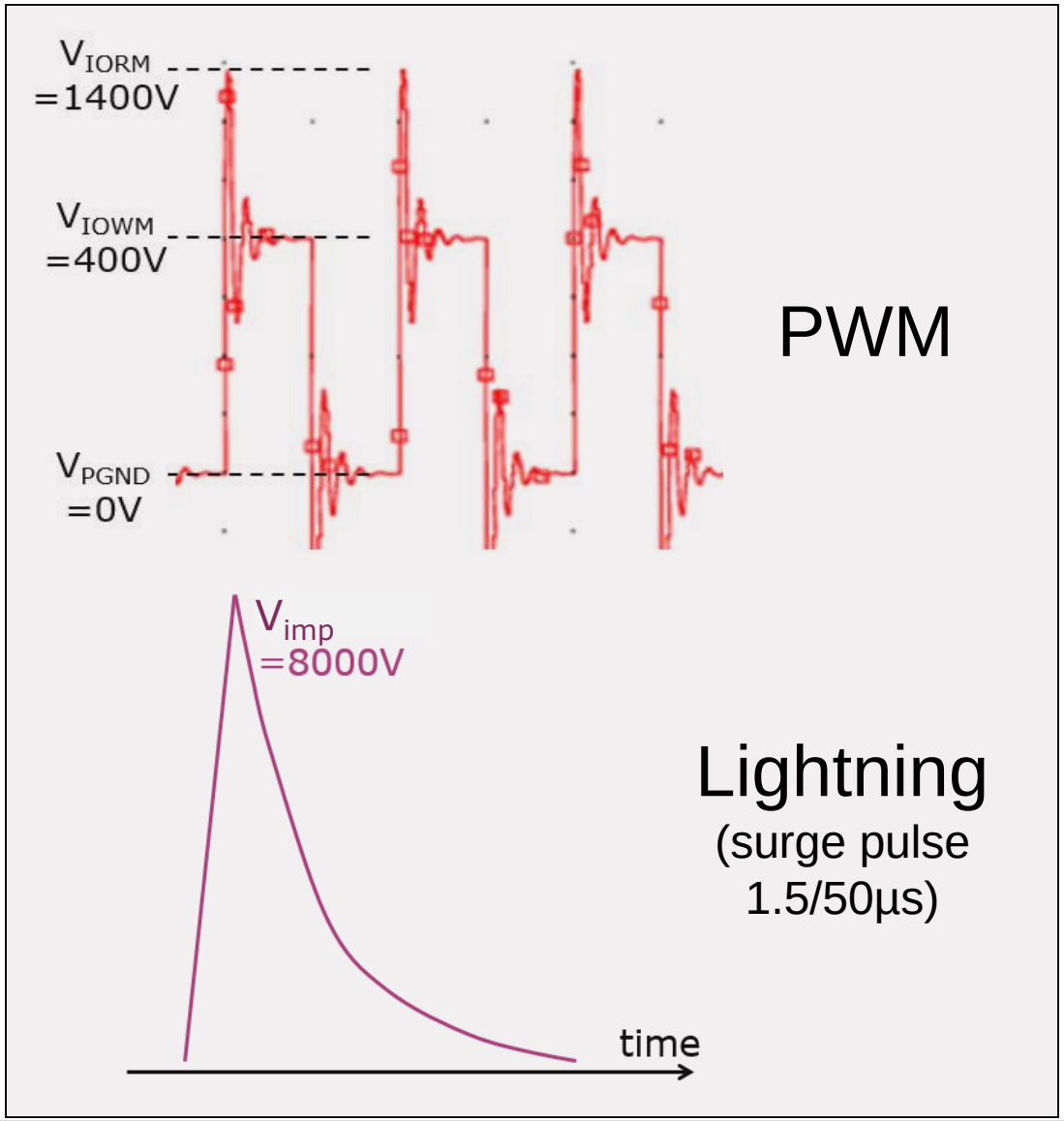
Overview

1. Introduction: Why are isolated gate-drivers needed?
2. Overvoltages occurring in power networks
3. Required Safe-Operating-Area (SOA) for gate-drivers
4. HV-HF requirements out of the IEC 60664-4
5. Typical construction of a magnetic/capacitance coupler
6. Breakdown behavior of dielectrics and their mathematical description
7. Breakdown mechanism in the low/medium voltage range:
   a. Partial Discharge
   b. Fowler Nordheim tunneling
   c. Mold compound breakdowns
8. Summary

Critical Voltages at the example of a Gate Driver



- V_{op} is the voltage due to the switching including its parasitic ringing and temporary overvoltages.
- V_{imp} (impulse voltage) is due to lightning on the transmission lines.



Overvoltages due to electrical disturbances (IEC-60364-4-44)

The following subclauses consider four situations as proposed in 442.1, which generally cause the most severe temporary overvoltages such as defined in IEC 60050-604:

- fault between the high-voltage system(s) and earth (see 442.2);
- loss of the neutral in a low-voltage system (see 442.3);
- accidental earthing of a low-voltage IT system (see 442.4);
- short-circuit in the low-voltage installation (see 442.5).

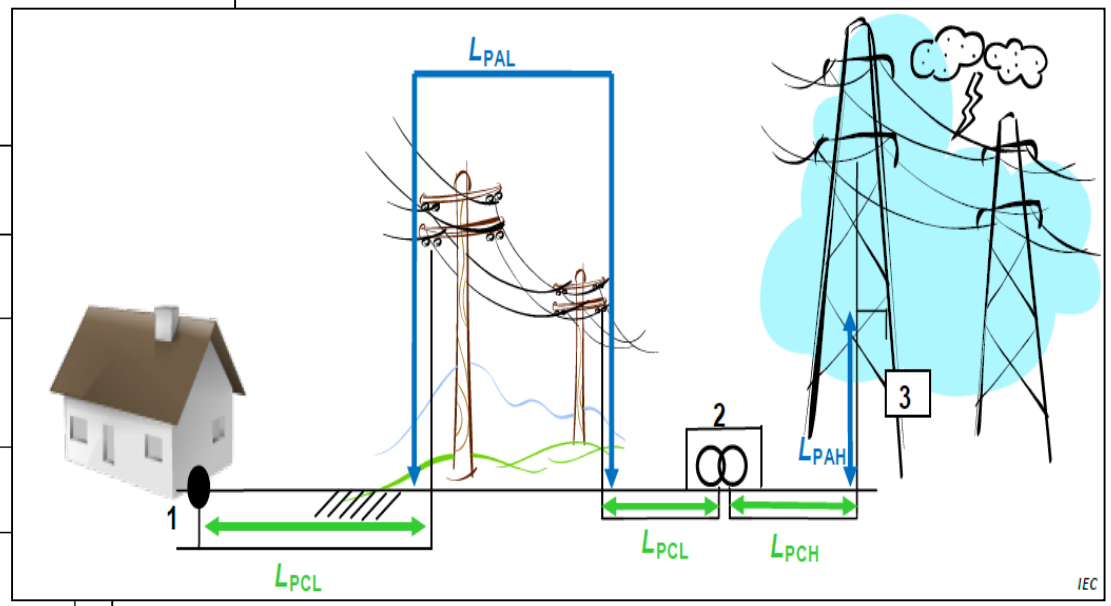


Table 44.A2 – Permissible power-frequency stress voltage

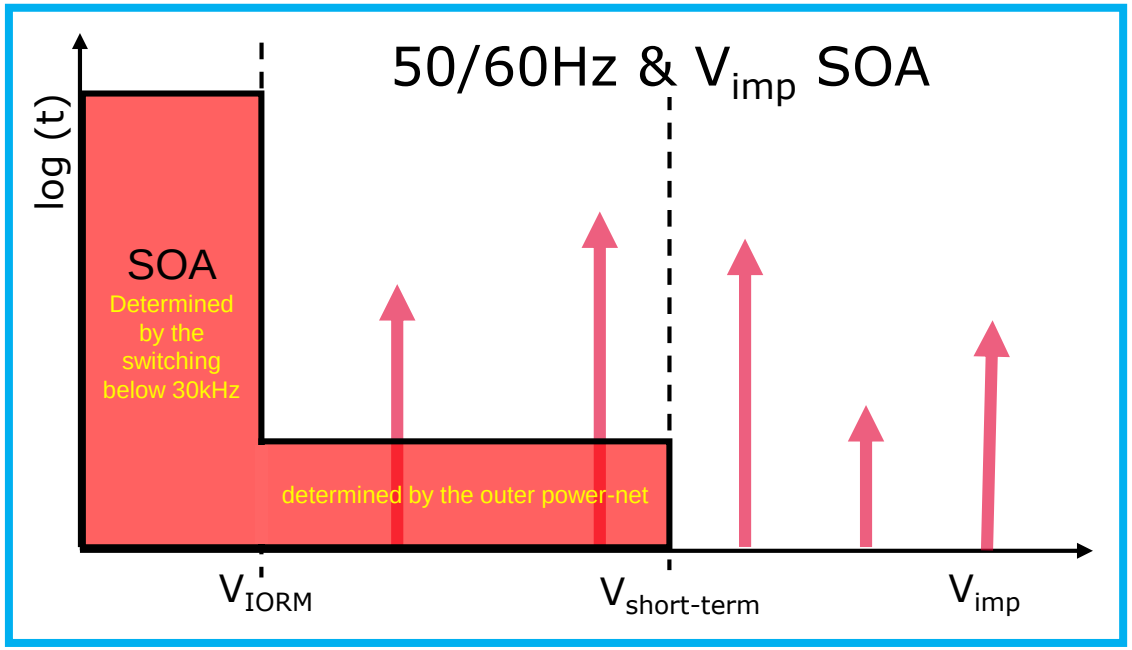
Duration of the earth fault in the high-voltage system *t*	Permissible power-frequency stress voltage on equipment in low-voltage installations *U*
>5 s	U_o + 250 V
≤5 s	U_o + 1 200 V

In systems without a neutral conductor, U_o shall be the line-to-line voltage.

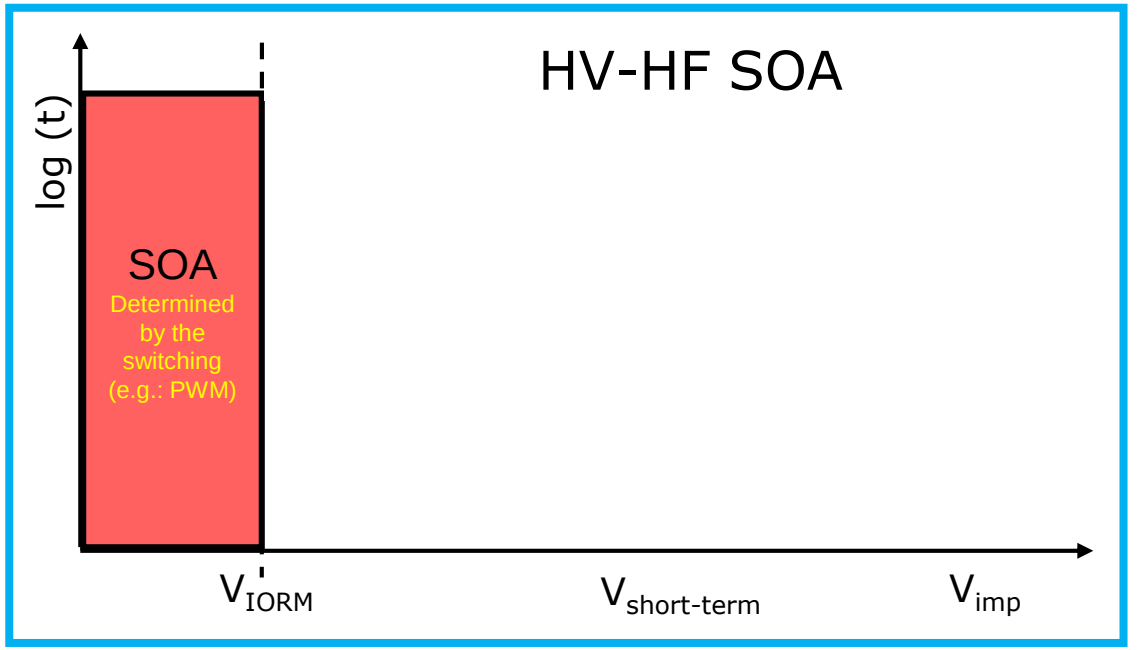
NOTE 1 The first line of the table relates to high-voltage systems having long disconnection times, for example, isolated neutral and resonant earthed high-voltage systems. The second line relates to high-voltage systems having short disconnection times, for example low-impedance earthed high-voltage systems. Both lines together are relevant design criteria for insulation of low-voltage equipment with regard to temporary power frequency overvoltage, see IEC 60664-1.

NOTE 2 In a system whose neutral is connected to the earthing arrangement of the transformer substation, such temporary power-frequency overvoltage is also to be expected across insulation which is not in an earthed enclosure when the equipment is outside a building.

Safe-Operating-Area

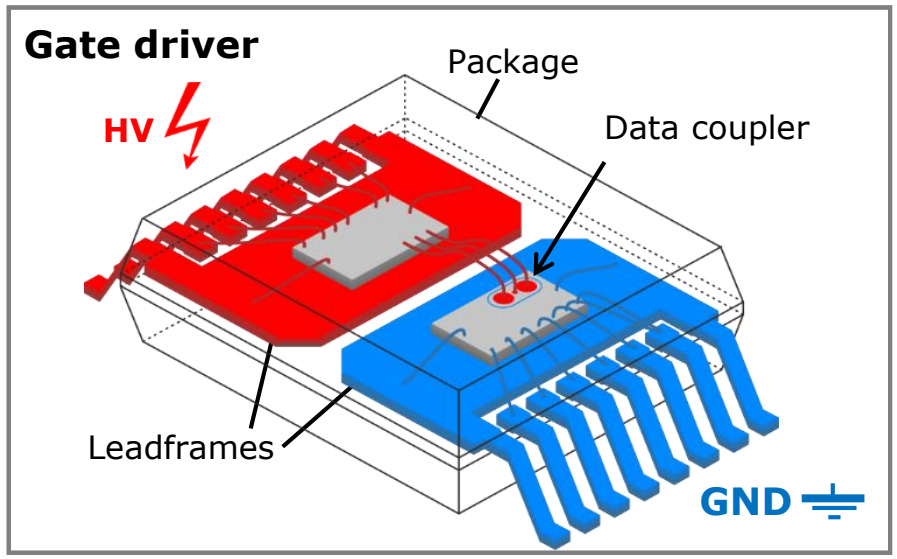


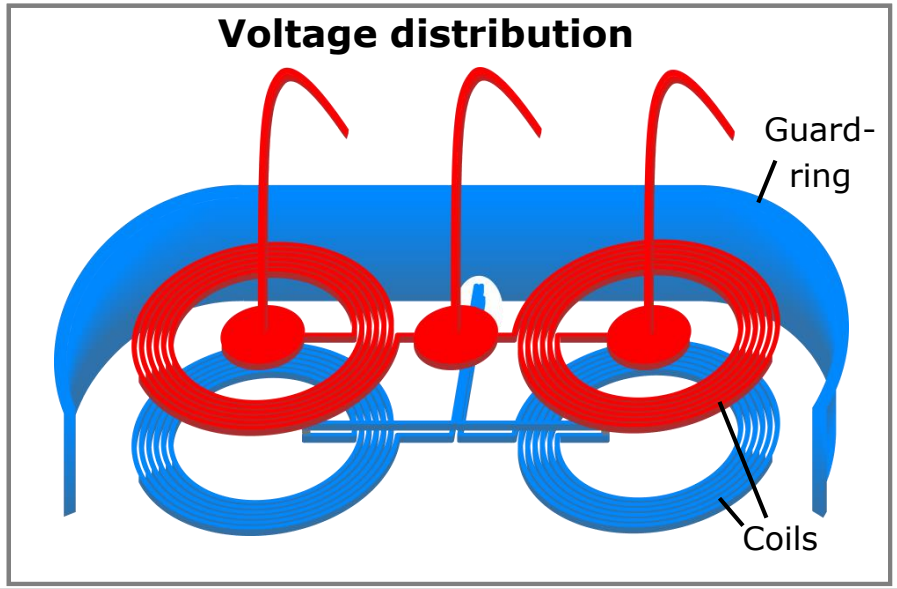
Surge pulses are marked with arrows. The number of surge pulses are not specified in any standard. They can occur at any voltage below Vimp.

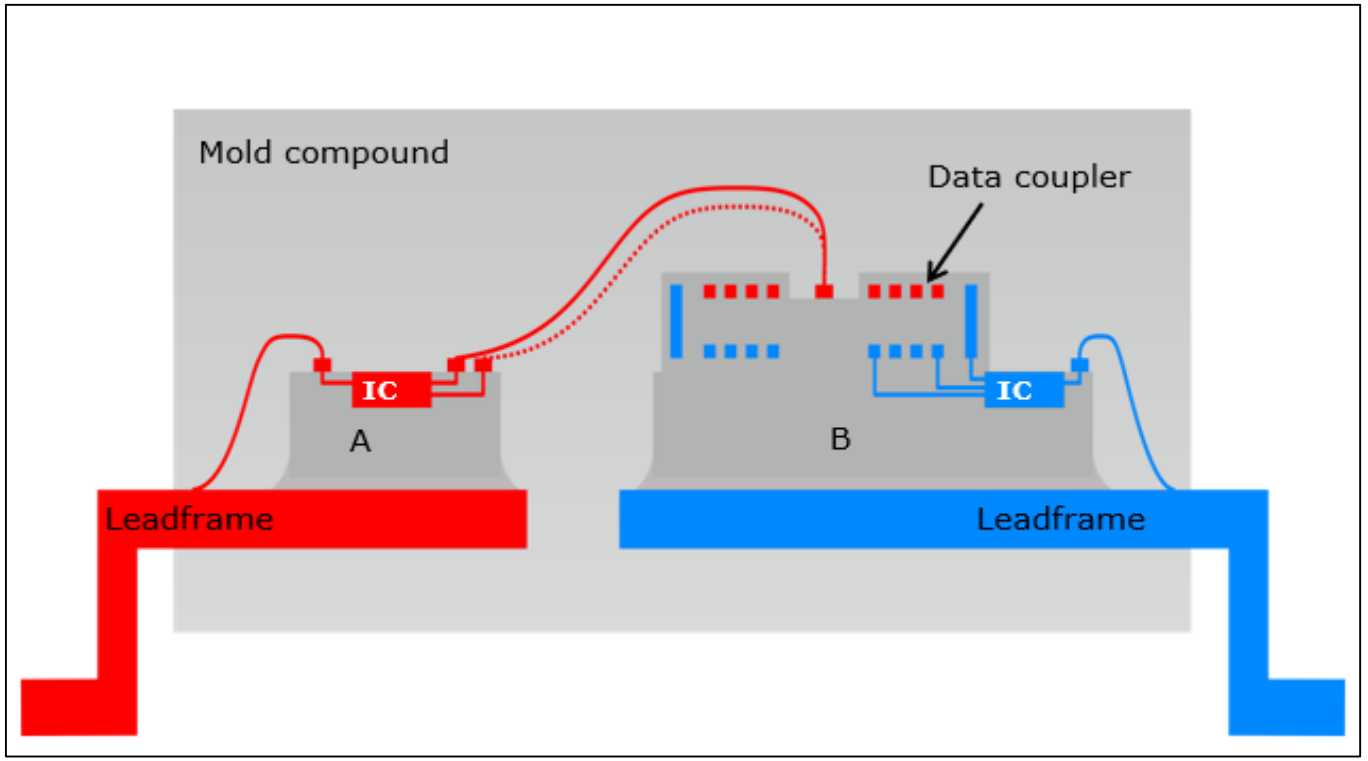


- The long-term and short-term overvoltages specified by the IEC 60664-1 have the power-net frequency.
- Switching power applications below 30kHz can be certified with tests running at 50/60Hz according to the IEC standards.
- But beyond 30kHz the standardization requirements are changing drastically.
- This concerns applications with CoolMOS, GaN and SiC power switches. Typically frequencies go up to 2MHz.
- Hence, the SOA for the couplers is falling into a part relevant for 50/60Hz and the surge pulse and into a HV-HF part.

Typical construction of magnetic coupler





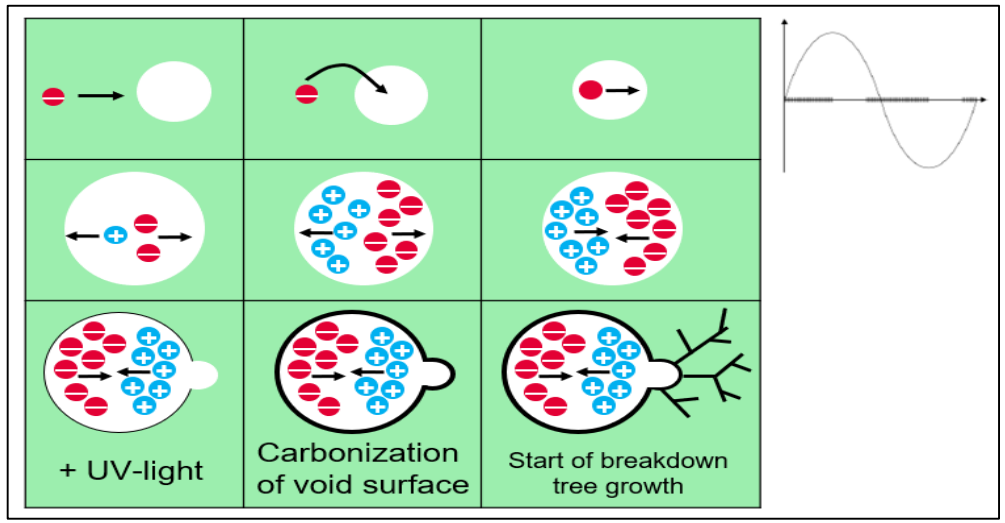


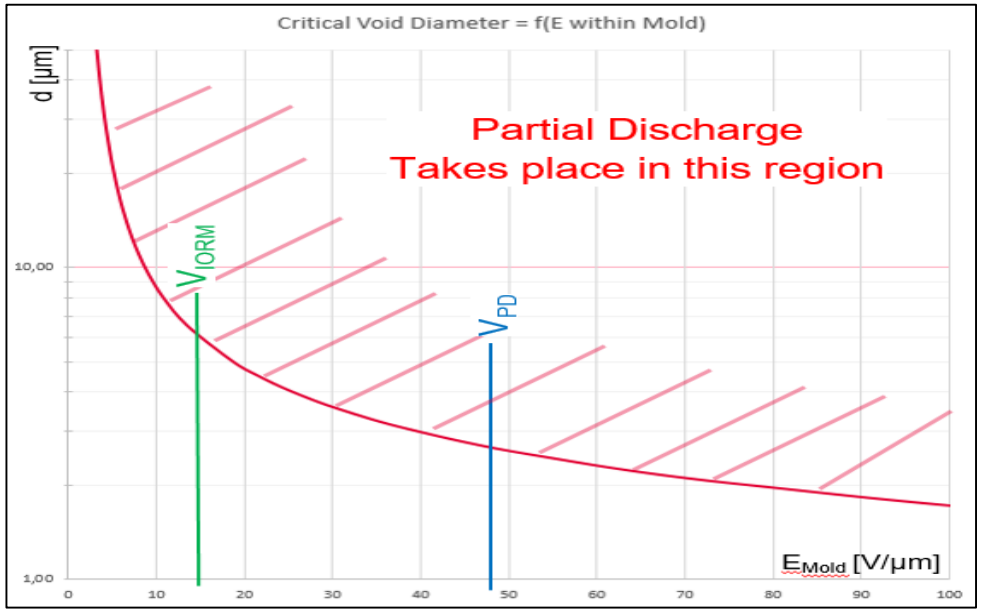
- Through a high voltage insulation barrier information and/or energy are transferred.

What is the standard IEC 60664-4 requiring for PWM switching frequencies above 30kHz?

- The IEC 60664-4 requires increased distances through insulations with increasing frequency. For example, an isolated gate-driver running at 200kHz would need twice the distance between the isolating coils as for a 30kHz application depending on the dielectric material. An increase by a factor of 5 is needed for 1MHz.
- Hence, the up to now used gate-drivers optimized for applications below 30kHz could not be used for the upcoming applications with GaN and SiC power-stages running at frequencies up to 2MHz. The isolation volume for such high frequency applications have to be drastically increased.
- On which basis does the IEC 60664-4 get to the conclusion of increased distance through insulation? The standard assumes:
  - that there is no threshold voltage and that already the avalanche part of the TDDB curve determines the total curve down to 0V,
  - that the only life-time limiting mechanism is the partial discharge,
  - → that there is a clear frequency dependency of the breakdown mechanism over the total voltage.

Does partial discharge has a threshold voltage?

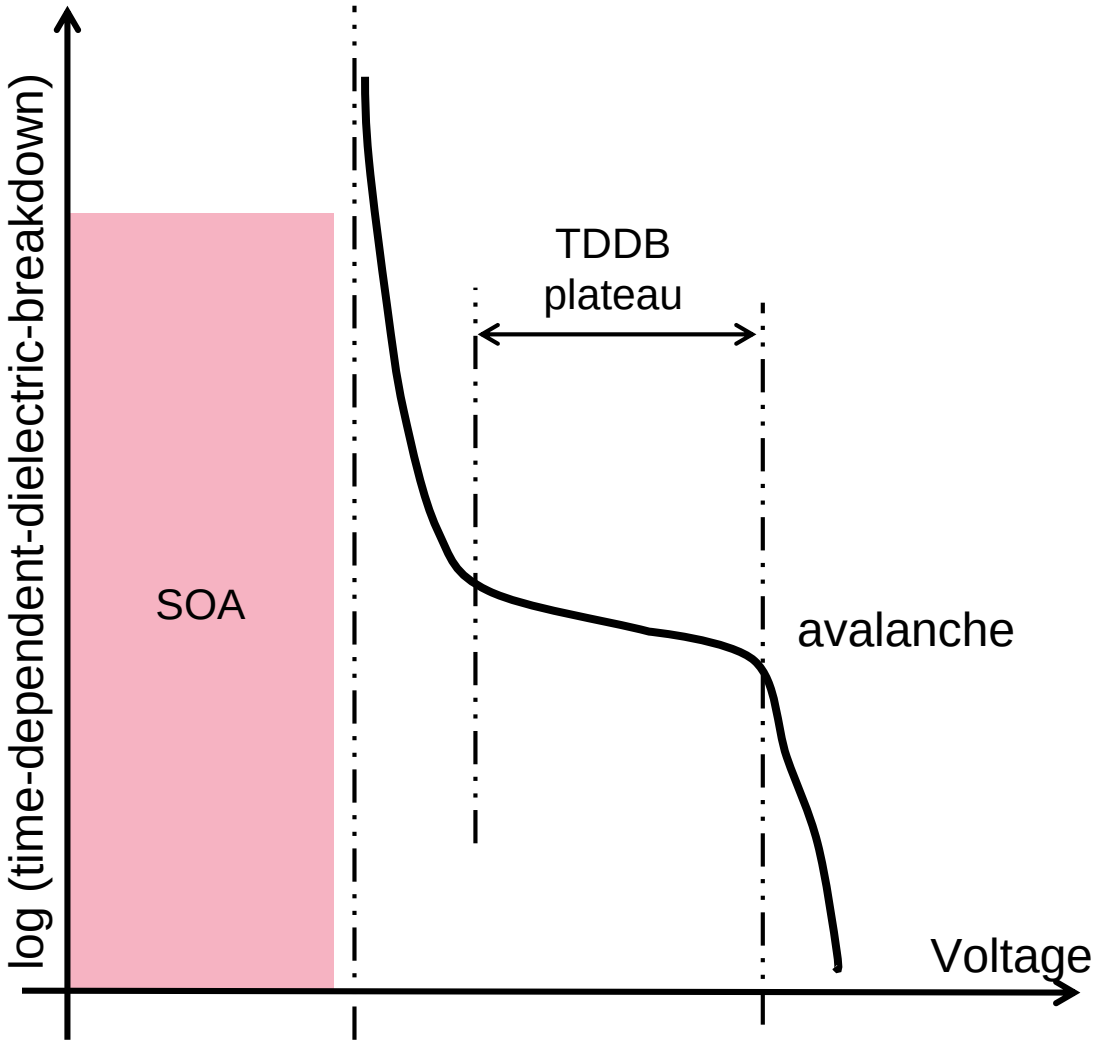




- To start partial discharge within a void, an electron has to be in the void.
- If the void is larger than the free path of the electrons inside the void filled with gas/air a plasma is ignited which can be measured from outside as partial discharge.
- The higher the e-field within the void the more electrons are generated (avalanche generation). This intensifies the plasma.
- A higher frequency of the e-field intensifies further the plasma/partial discharge.
- The plasma can generate UV-light which further degrades the void surface.
- The degradation speed is proportional to the frequency.

- If the void is smaller than the free path, no plasma/partial discharge occurs, even if the frequency increases drastically.
- → Partial discharge has a threshold voltage below which the degradation due to partial discharge stops!

Typical Time-Dependent-Dielectric-Breakdown behavior over voltage



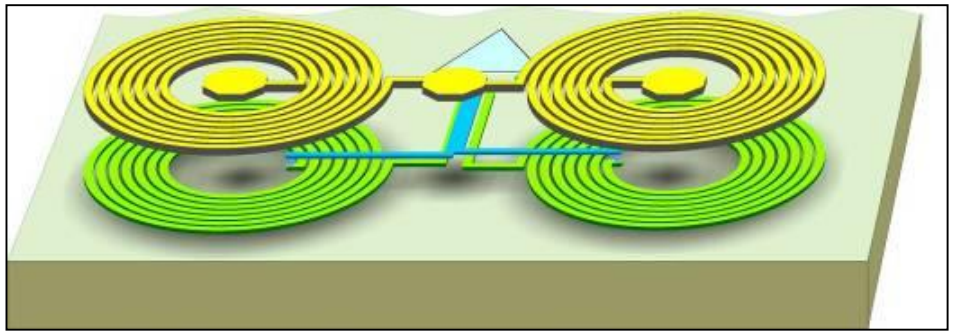
- All dielectrics show a threshold voltage below which the failure mechanism is not taking place.
- Below the threshold voltage the life-time becomes infinity. Ideally the maximum voltage of the SOA should be in the best case smaller than this threshold voltage.
- The degradation mechanism in the TDDB plateau region is determined by partial discharge, space charge degradation, Fowler-Nordheim tunneling in combination with trap generation.
- Hence, it is **not** possible to use the failure data out of the avalanche region for determining the threshold voltage.

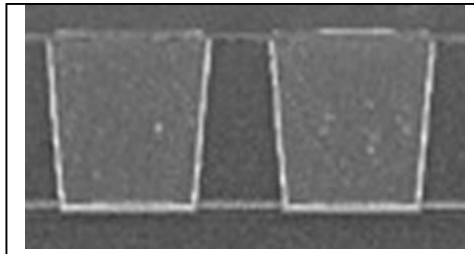
General equation to describe the growth of the 1st tube of a breakdown tree

$$t_I \times f \times (G_n - G_{th}) = C_t$$

- t_I: Initiation time
- f: frequency
- G_n: energy from injection/extraction current
- G_{th}: energy input required for damage
- C_t: energy proportional to accumulated damage required to give 1st tube

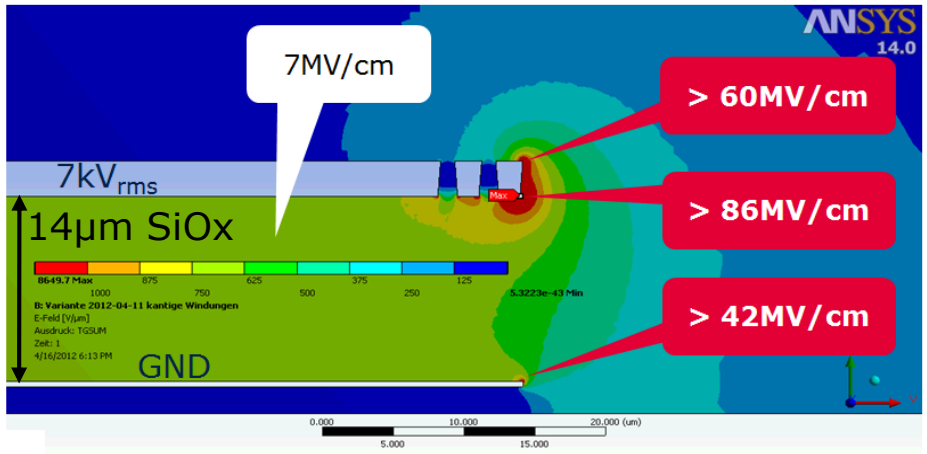
What about our SiO between the coils?



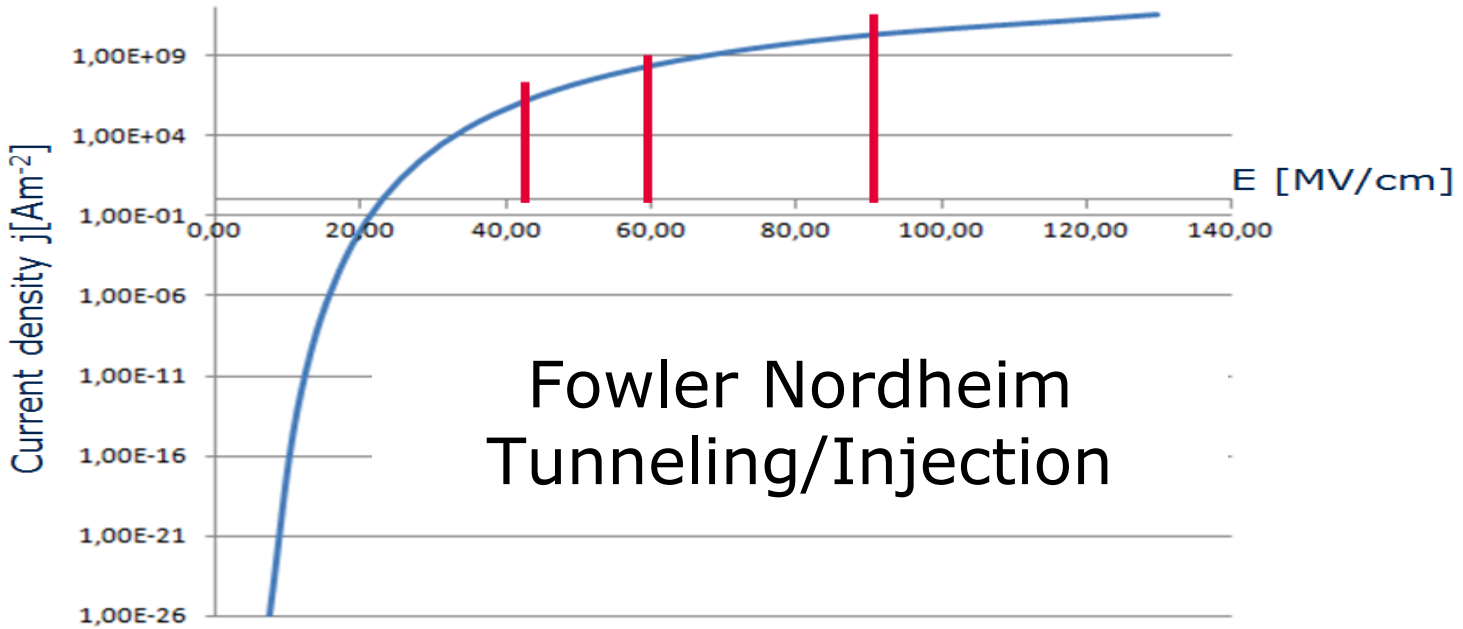


Metal-cross-section of top and bottom metal of transformer have sharp corners!

Curvature radius of metal corners was assumed to be 1nm!

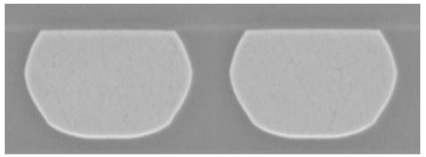


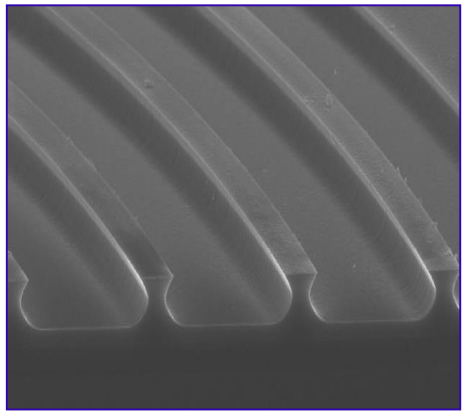
- At the sharp corners of the metal cross-sections the local E-field is enormous resulting in a large Fowler Nordheim injection current which determines the life time of the SiO.
- But below 5MV/cm the FN-tunneling becomes negligible. This would be threshold e-field. → $V_{th} \approx 0.4kV_{rms}$

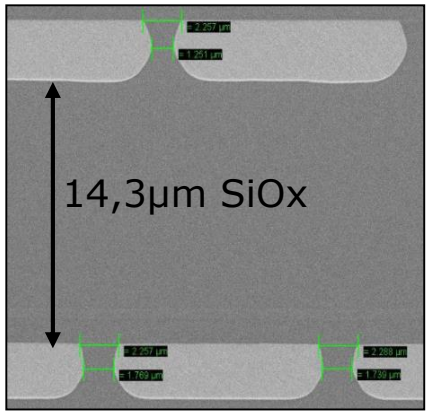


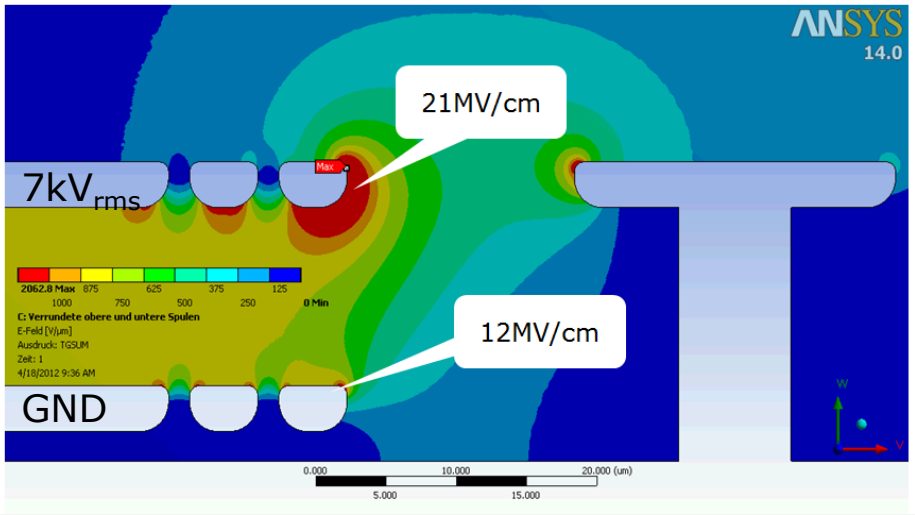
Reliability improvement by round cross-sections Improvement by a factor of 10!

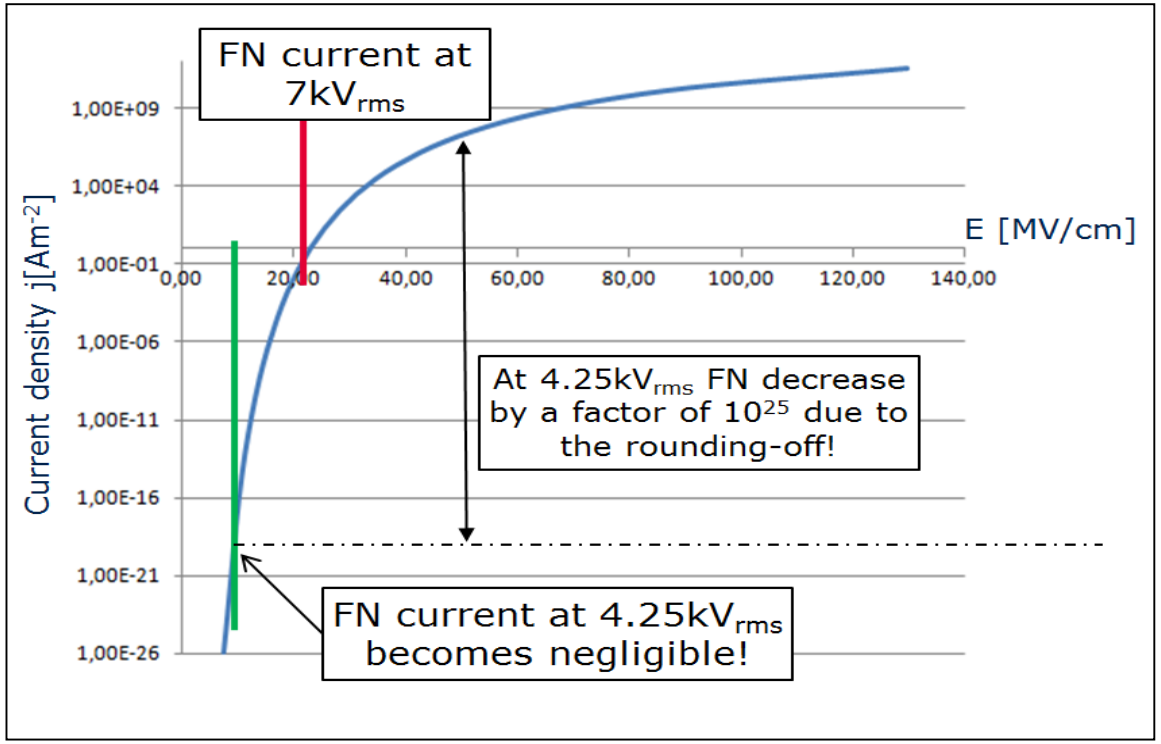
Cross-section of metal lines is rounded-off!





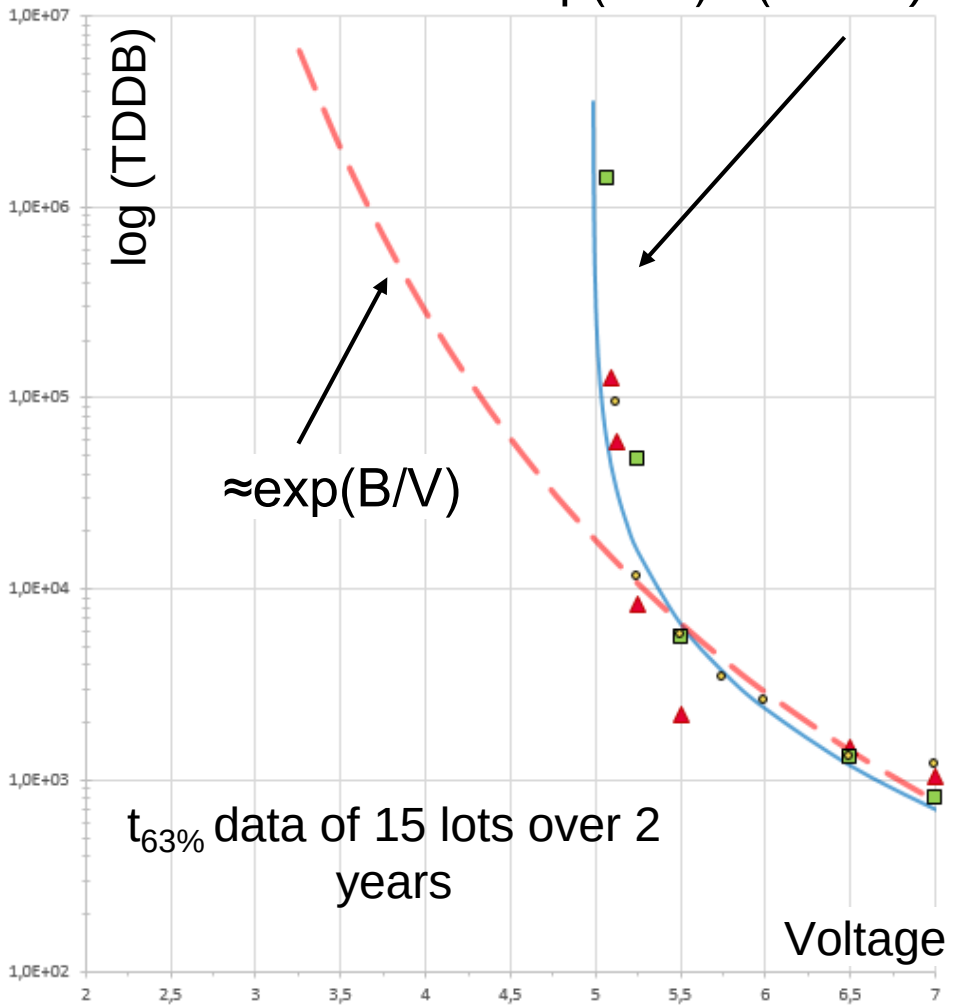






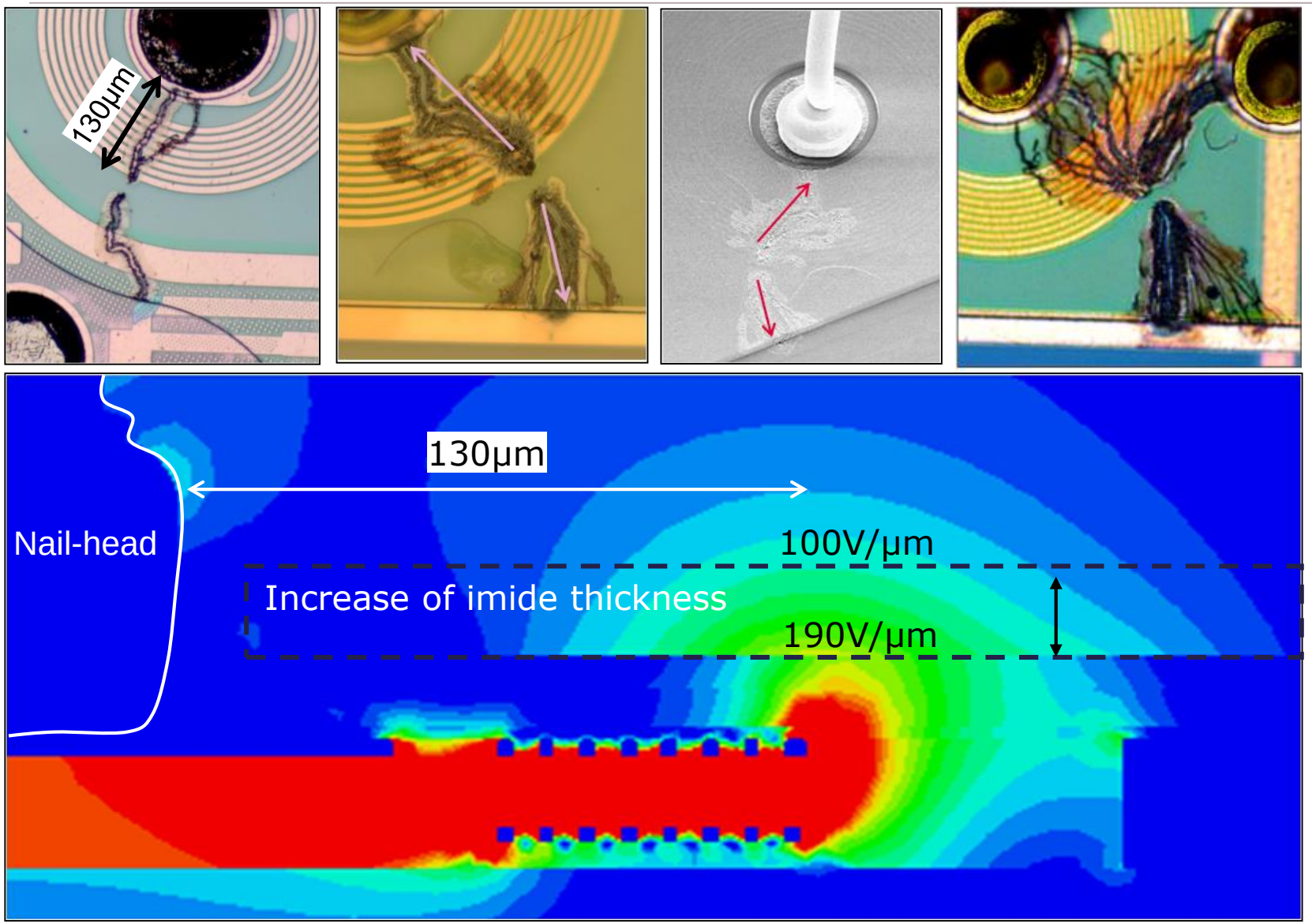
- By rounding-off the sharp corners of the metal lines the e-field is reduced so drastically that below 4.25kV$_{rms}$ the FN injection current diminishes totally.
- The FN-injection current has a threshold voltage, below which it has no influence anymore on TDDB.

SiO Breakdowns



- Applying the 1st tube equation t_l x f x (G_n –G_{th}) = C_t in combination with FN-equation results in
  - $t_l \approx \exp(B/V) / (D-1/V)$
- The approximation with just L = A * exp(B/V) does not work at all.
- A threshold voltage has to be introduced: L= A * exp(B/V) / (D-1/V) with 1/D ≈ 5kV_{rms}.
- The time dependency exp(B/V) just maps the trap generation via hot electrons which is proportional to exp(-B/V).
- But the trap generation due to electrons injected by FN-tunneling has a threshold e-field/voltage.
- Below this e-field even in the case of very high frequencies no damage is generated.

1st tube generation at the interface imide/mold



- 1st breakdown tube is generated at the imide/mold interface.
- Therefore, no breakdown marks are found on the chip surface below this tube.
- This starting point is far away from the electrodes.
- We assume that the electrons are getting out of the traps located at the imide/mold interface.
- The trap depth again defines the threshold e-field/voltage below which no degradation takes place even if the frequency is drastically increased.

Derivation of initialization time t_I at the imide/mold interface

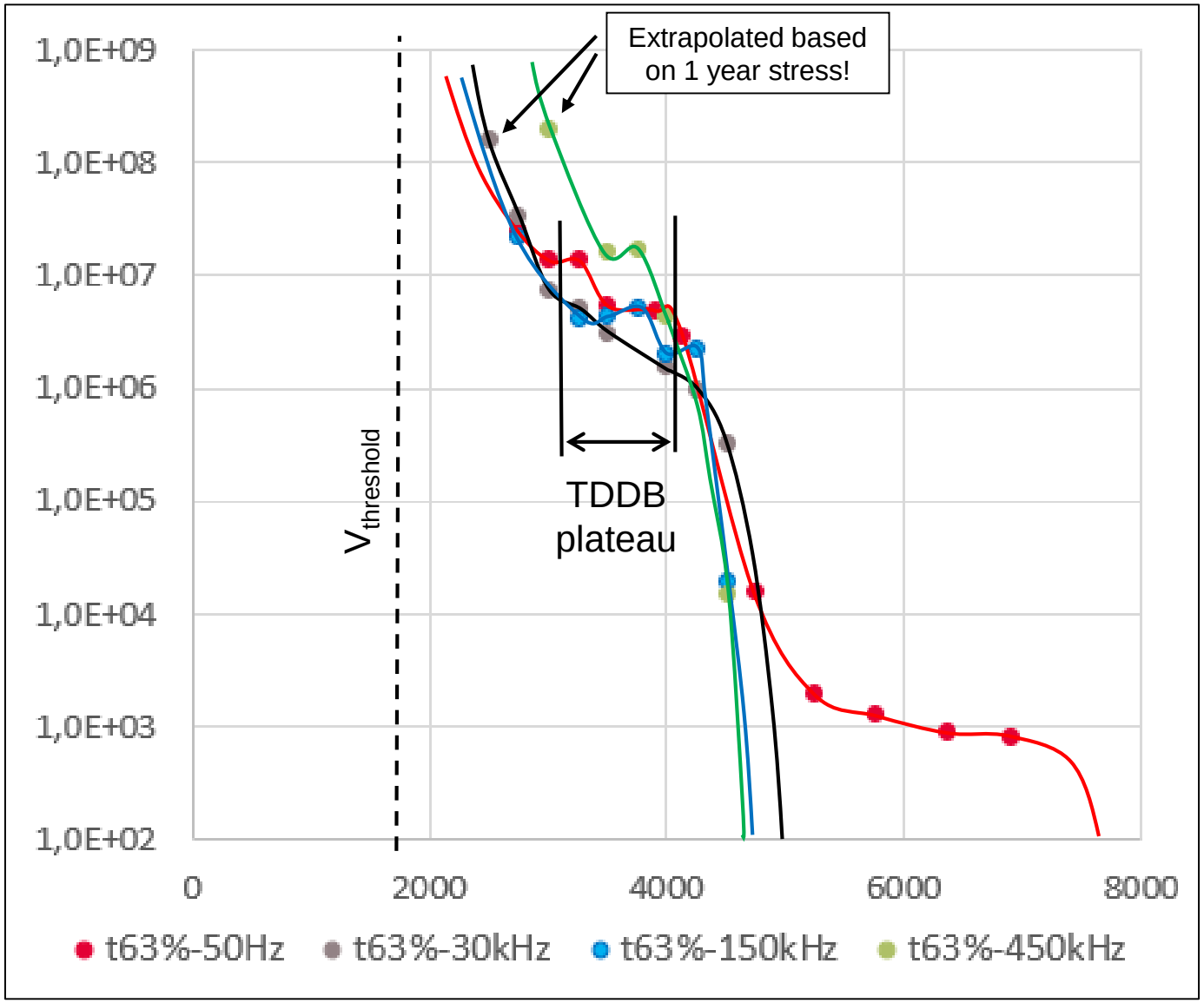
$$f * ti * (Nq * Eexp\left(A\sqrt{E} - B\emptyset_B\right) * \exp\left(-\frac{B}{E}\right) * E - Gth) = Ci$$

Poole-Frenkel current via traps

Impact ionization in solids

➔ $t_{I\text{-}SP} \approx (C/f) \exp(B'/V) / V^2$ for $G_{th} \rightarrow 0$

Voltage/Frequency/SiO-&Imide-Thickness Dependency



- In contrast to the high voltage region the frequency dependency in the TDDB plateau region becomes negligible.
- Just for 450kHz the TDDB plateau height increases as also the threshold voltage. Infrared measurements of the devices under stress show that the outside temperature is drastically increased. This is due to dielectric losses.
- The breakdown threshold voltage of the mold is also increased with thicker imide leading to smaller e-fields at the imide/mold interface. Measurements of thick imide devices at 30kHz showed a comparable TDDB plateau.
- The threshold voltage at 30kHz for the thicker imide samples is around $3kV_{rms}$. The Vth improvement of the thicker imide is about $1kV_{rms}$.

Summary

1. The breakdown mechanism at high voltages is determined by avalanche generation and shows a clear frequency dependency which is correctly stated in the IEC 60664-4.
2. But the breakdown mechanism in the medium voltage range relevant for PWM SOA shows a threshold e-field/voltage for Fowler-Nordheim injection, partial discharge and interface de-trapping at the imide/mold interface.
3. For frequencies up to 150kHz, the frequency dependency becomes negligible the closer the stress voltage gets to the threshold voltage.
4. If the frequency is increased further (450kHz) the threshold e-field/voltage is also increasing. This is probably due to dielectric losses increasing the temperature within the devices. This decreases the free path of the electrons. This effect is also known from silicon. Experiments at 800 and 1800kHz show consistent results.
5. → Isolating gate-drivers do not need larger distances through insulations with increasing frequencies as required in the IEC 60664-4.

→ The IEC 60664-4 has to be rewritten! ←

Part of your life. Part of tomorrow.