IRSP 2023

Bad Schandau

Jun.-Prof. Dr.-Ing. Iuliana Panchenko, Fraunhofer IZM ASSID and TU Dresden I 25.04.2023

Hybrid bond and nanowired bump technologies for high density interconnect formation on wafer level

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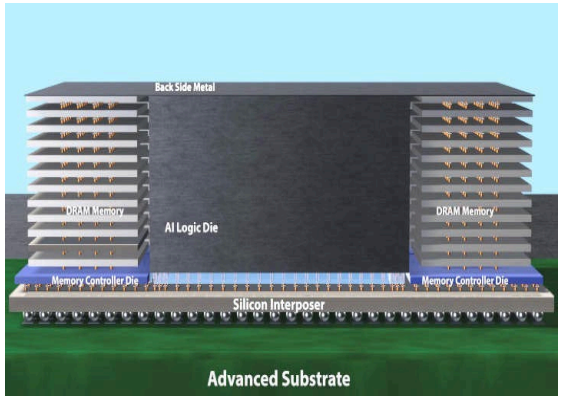
Content

Introduction

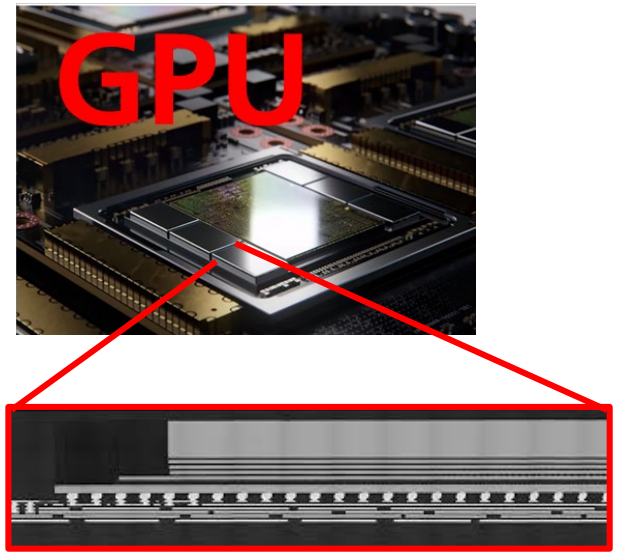
Application field for fine-pitch interconnects

- Advanced 3D / 2,5D integration with fine-pitch interconnects and TSVs in all high-performance application areas:
  - Stacking of memories
  - CMOS image sensors (stacked sensor and image processors)
  - Graphic processor units
  - All next generation devices
- Main Drivers:
  - High I/O number, perfect electrical performance (high signal velocity, low losses), low power
- Next integration solutions:
  - Chiplets (high yield with small chiplets, I/O pitch between 0,1 to 10 µm, package level integration, standardized surfaces)

Ref: Sony, CIS



Ref: Applied Materials and BESI



Ref: NVIDIA, Pascal GPU

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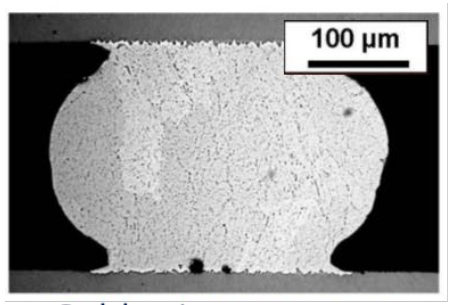
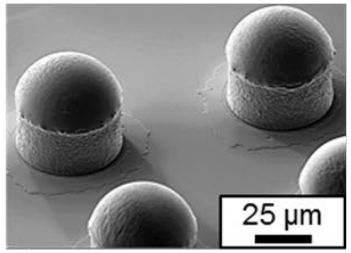
Introduction

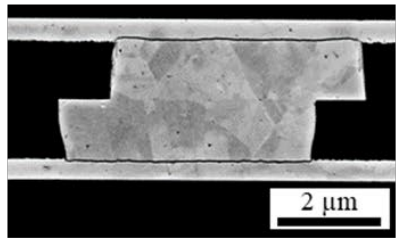
Scaling of interconnects and new material interaction



Solder interconnect
(BGA to WL/CSP)
Ø 800 - 250 µm



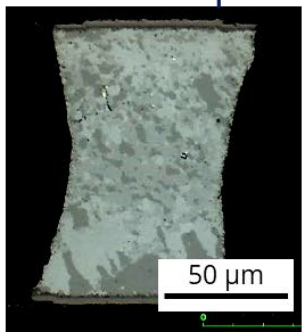
Cu-Pillar
Ø 50 - 20 µm



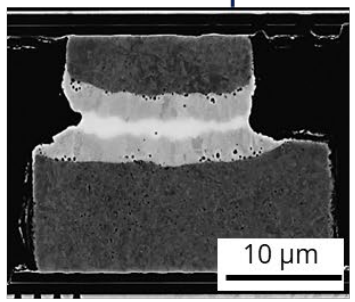
Hybrid bond Cu/SiO_2
Ø 10 - 1 µm

500µm **50µm** **5µm** **nano**

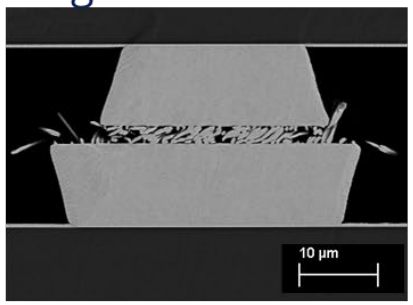
Flip Chip
Ø 90 - 25 µm



SLID interconnect
Ø 25 - 7 µm



Nanowire bumps (Ø 20 – 1 µm)
Ø single wire 400 – 10 nm



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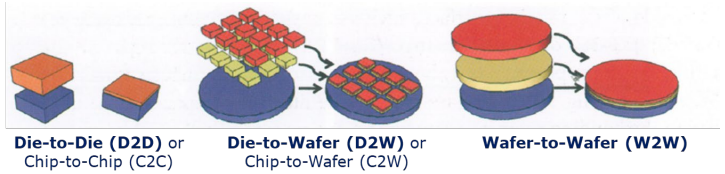
Introduction

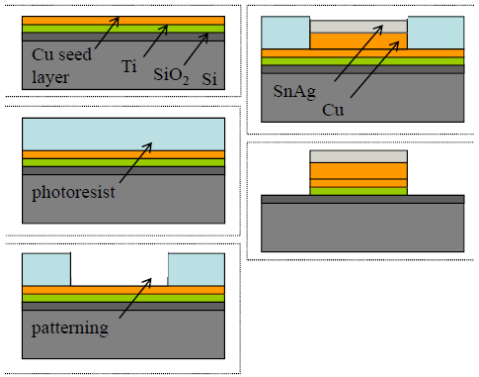
Classification of interconnect technologies



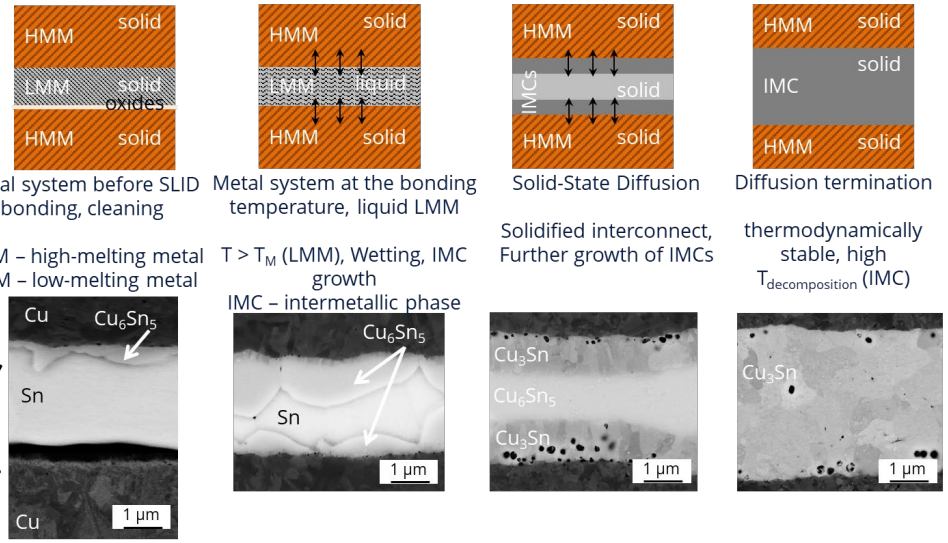
- Interconnect technologies
  - Die-to-Substrate
    conventional technologies (pitch > 100 µm)
    - Wire bonding
    - Flip-chip bonding (soldering)
    - Tape automated bonding
    - Conductive adhesive
  - D2D, D2W, W2W
    stacking technologies (pitch < 100 µm)
    - Direct bonding, Cu/Cu TCB
      - No passivation
      - With passivation
        - SAM
        - SAB
    - Cu/Cu with interlayer
      - SLID
      - Cu-pillar
    - Hybrid bonding or DBI (Cu/SiO_2)
    - Nanobonding
      - Reactive bonding
      - Nanoparticle-sintering
      - CNTs
      - Nanowired bump and film
      - Nanoporous interconnects

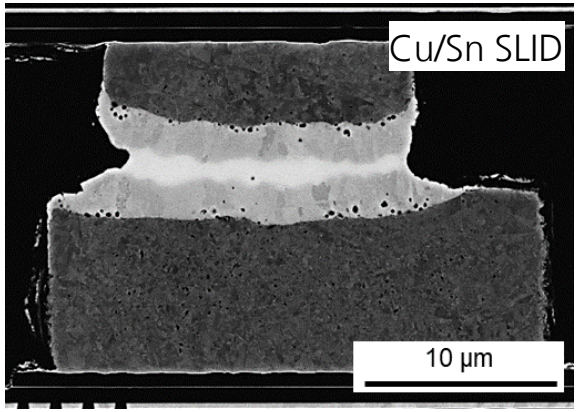
Introduction

Solid Liquid Interdiffusion Bonding (SLID) – State of technology



- Barrier and seed
- Lithography
- ECD Cu and SnAg
- Strip and wet etch
- Reflow only for larger caps





Ref.: Panchenko, PhD, 2013

- IMCs: Cu_6Sn_5, Cu_3Sn
- Porosity and voids:
  - Destannification
  - Kirkendall voids
  - Processing
  - Volume phase shrinkage

→ **Potential reliability risk**

Parameter	Value
sizes	Ø 7 to 30 µm
pitches	15 to 60 µm
metals	Cu, Sn, SnAg, In, Au
activation	Clean, flux
atmosphere	Air

- POR process for customer die stacking
- Miniaturization → current work on µBump ø 5µm

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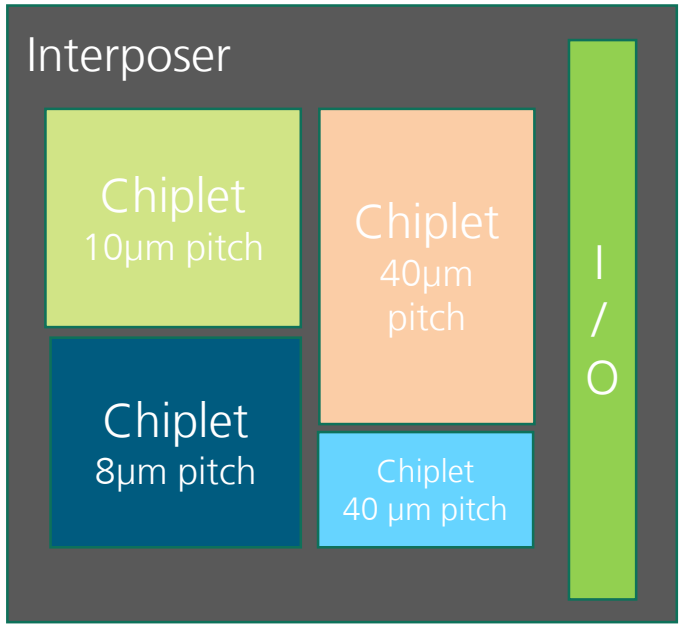
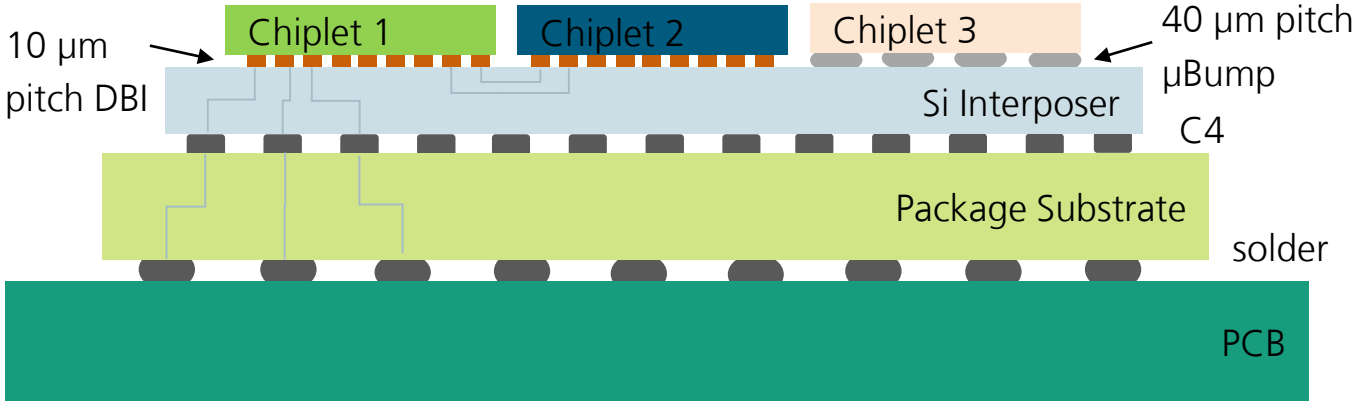
New Challenges

Chiplet integration and requirement of interconnect type and pitch combination





Combination of:

- Large and small interconnect and pitches (<10µm vs. 40µm pitch) for first level
- Different bonding technologies (hybrid bond vs. µbump)

→ Need for one appropriate interposer surface (all hybrid bond surface?)
→ Need for aligned assembly process (first assembly hybrid bond, after µbump?)

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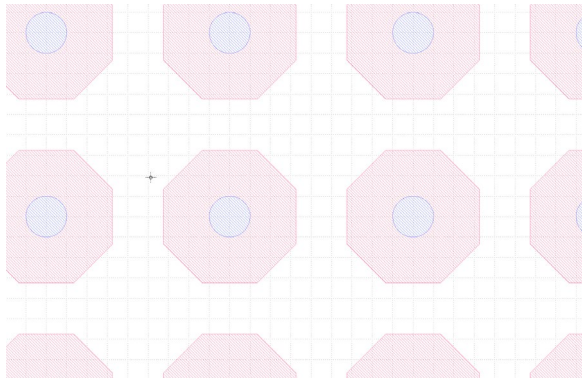
Hybrid Bond Interconnect

Hybrid bond interconnects

Hybrid bond advantages and requirements

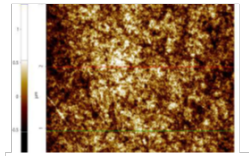
Advantages:

- W2W and D2W/D2D stacking
- Single metal (Cu)
- High reliability
- Mechanical encapsulation (SiO_2)
- Multiple stacking possible

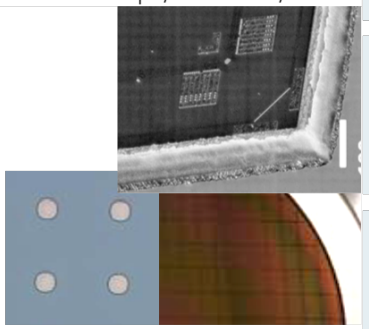


Test design: Ø 4 µm, 18 µm pitch

Requirements:

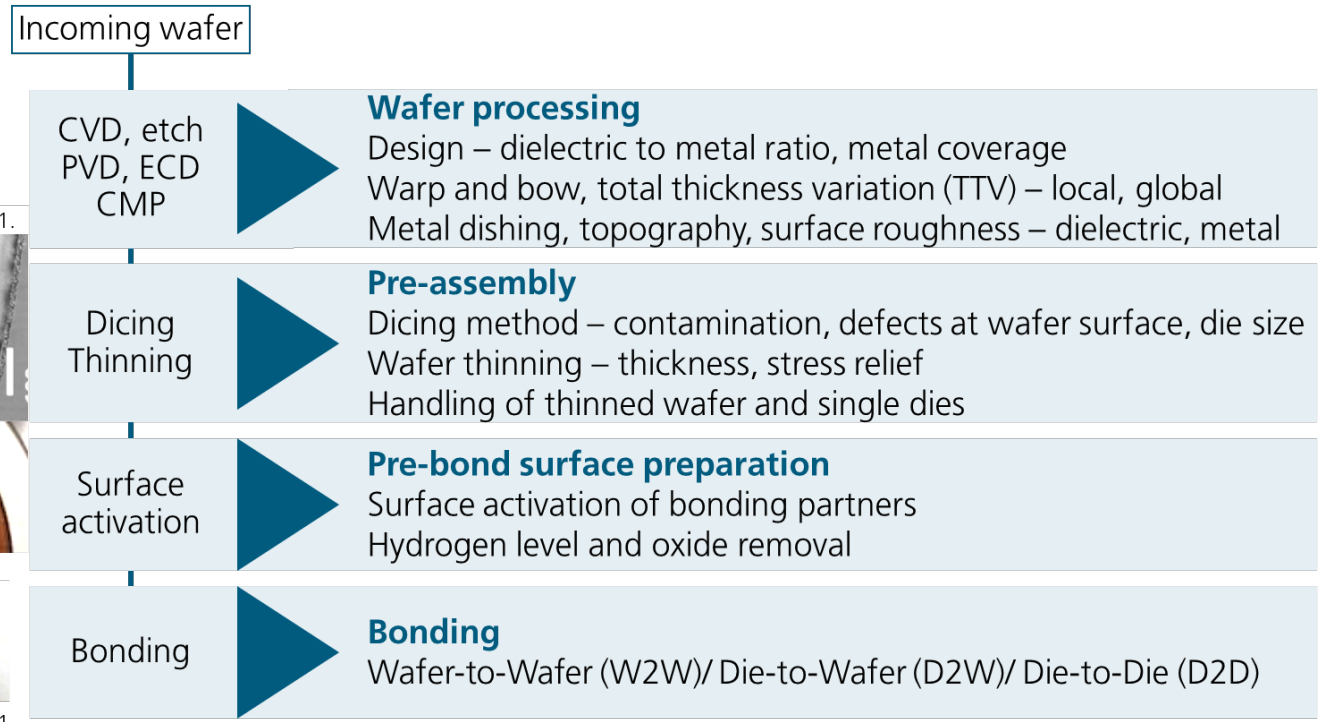


Ref.: C. Rudolph, Proc. ECTC, 2021.



Ref.: G. Gao, Proc. ECTC, 2019.

Ref.: C. Rudolph, Proc. ECTC, 2021.

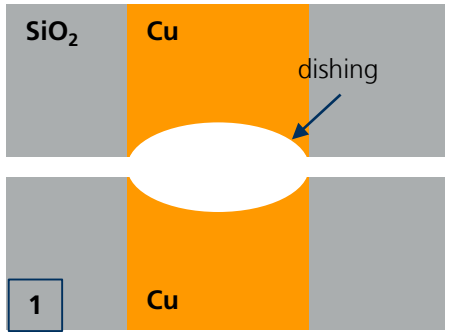


Ref.: Wenzel L., 3D Summit, 2022

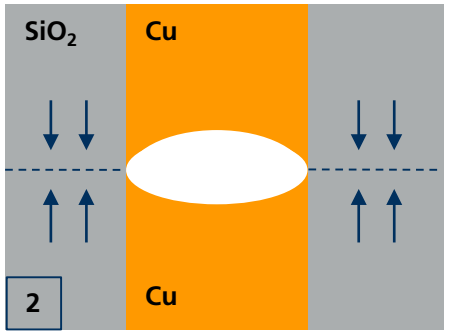
Hybrid bond interconnects

Bonding principles

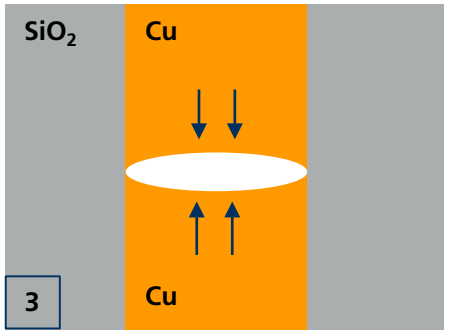
Surface preparation:
CMP → planarity, Cu dishing (few nm), oxide free

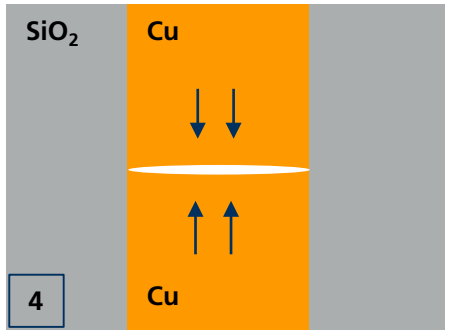


Step 1 (Oxide Bonding):
SiO_2-to-SiO_2, ($T_{bond} \approx 150°C$) bond

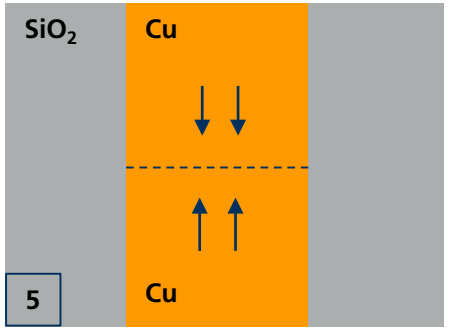


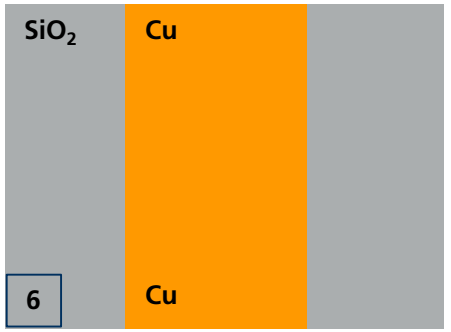
Step 2 (Cu-anneal):
Cu-to-Cu ($T_{bond} \approx 300°C$)
Cu expands and comes into contact



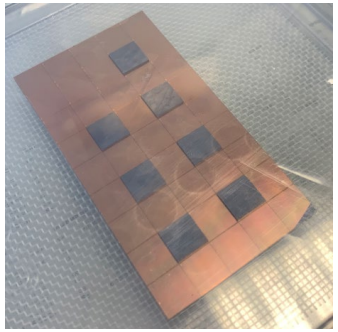


Cu-to-Cu interdiffusion with longer annealing,
Cu grains grow





Dies bonded via hybrid bonding



Typical bonding parameters:

- wafer-to-wafer bonding
- 150 °C for oxide bonding
- 300 °C anneal for Cu/Cu diffusion (hours)
- no additional bonding pressure necessary

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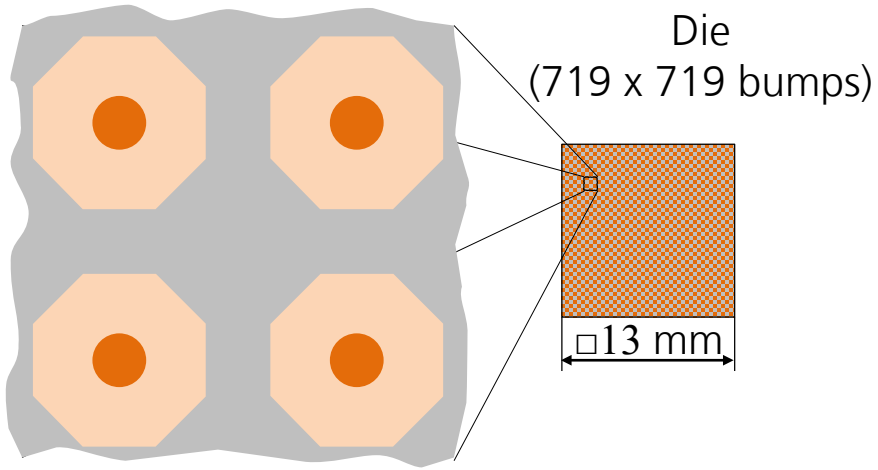
Hybrid bond interconnects

Experimental procedure



→ Wafer-to-Wafer Bonding (∅ 300 mm) with a 2-step profile (EVG Gemini):

- 150 °C (SiO_2 bond)
- 300°C (Cu anneal)

→ Electrical test

→ Dicing into small stacks (13x13) mm²

→ Reliability testing

→ Analysis (SEM and EBSD)

TABLE I
OVERVIEW OF INVESTIGATED RELIABILITY TEST CONDITIONS AND THE ASSOCIATED NUMBER OF INTERCONNECTS

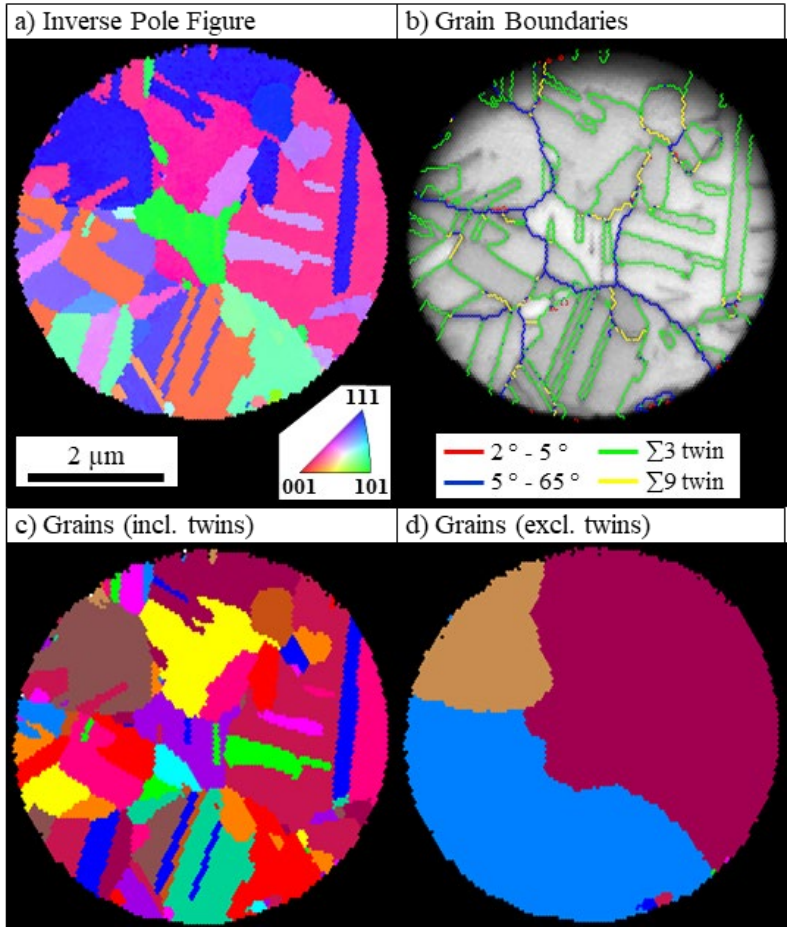
State	Conditions			EBSD
	Temperature	Medi-um	Cycles / Time	No. of investigated interconnects
Before bond.	-	-	-	16 (top view)
After bond.	150 °C (2h) + 300 °C (2h)	-	-	10 (cross-section)
TST	-40 °C / +125 °C (15 min dwell time)	air	1000 cycles	10 (cross-section)
HTS	150 °C	air	1000 h	10 (cross-section)
HTS	300 °C	N_2	0,5; 1; 3; 6 h	10 (cross-section)
HTS	400 °C	N_2	0,5; 1; 3; 6 h	10 (cross-section)
Mult. bond. cycles	One cycle: 2h @ 150°C + 2h @ 300°C, cool to 25 °C	N_2	2 to 9 cycles	10 (cross-section)

Ref.: Panchenko I., IEEE trans., 2022

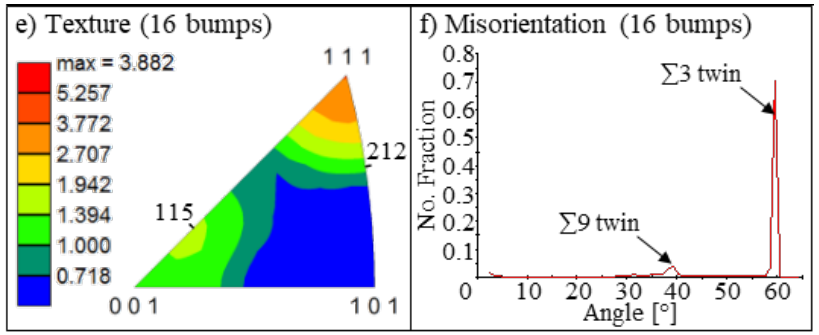
Hybrid bond interconnects

EBSD investigation of the Cu pads after CMP

⊙
in ND
[001]



Ref.: Panchenko I., IEEE trans., 2022

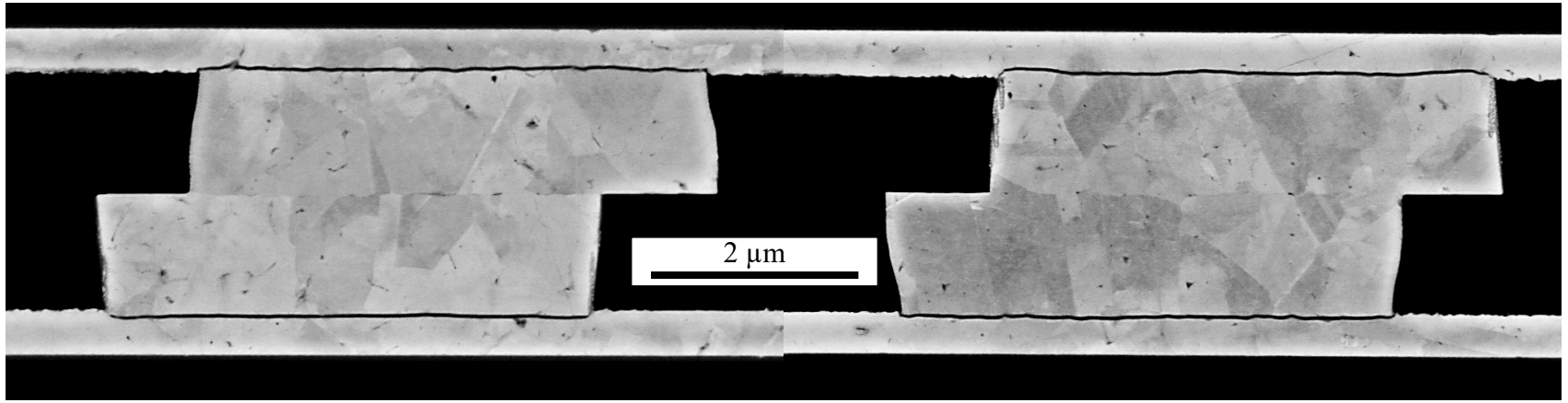


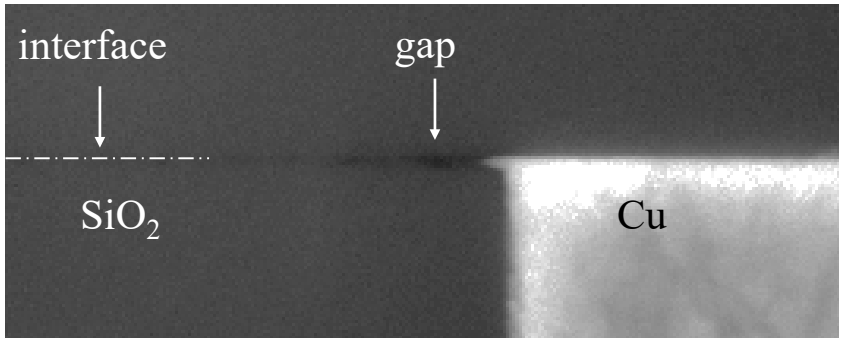
- mainly Σ3 and Σ9 twin boundaries
- Cu bump Ø 4 µm surface consists of only a few large grains (by excluding twins)
  - How many grains if we scale the hybrid bond further?
- average grain diameter is 1.02 µm
- {111} as a main texture with a smaller fraction of {115}

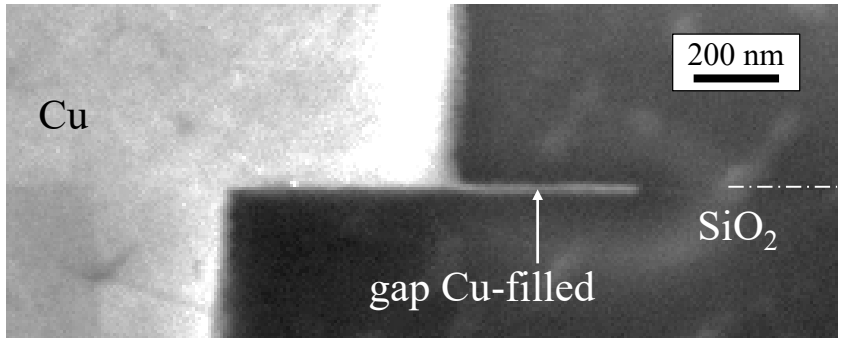
Σ3: 60° around <111> with {111} as twin plane
Σ9: 39° around <110> with {110} as twin plane

Hybrid bond interconnects

As bonded state: SEM







Seamless bonding interface → intergrowth of the Cu grains?

Some interconnects showed gaps filled with Cu on the edges (only preparation effect?

Ref.: Panchenko I., IEEE trans., 2022

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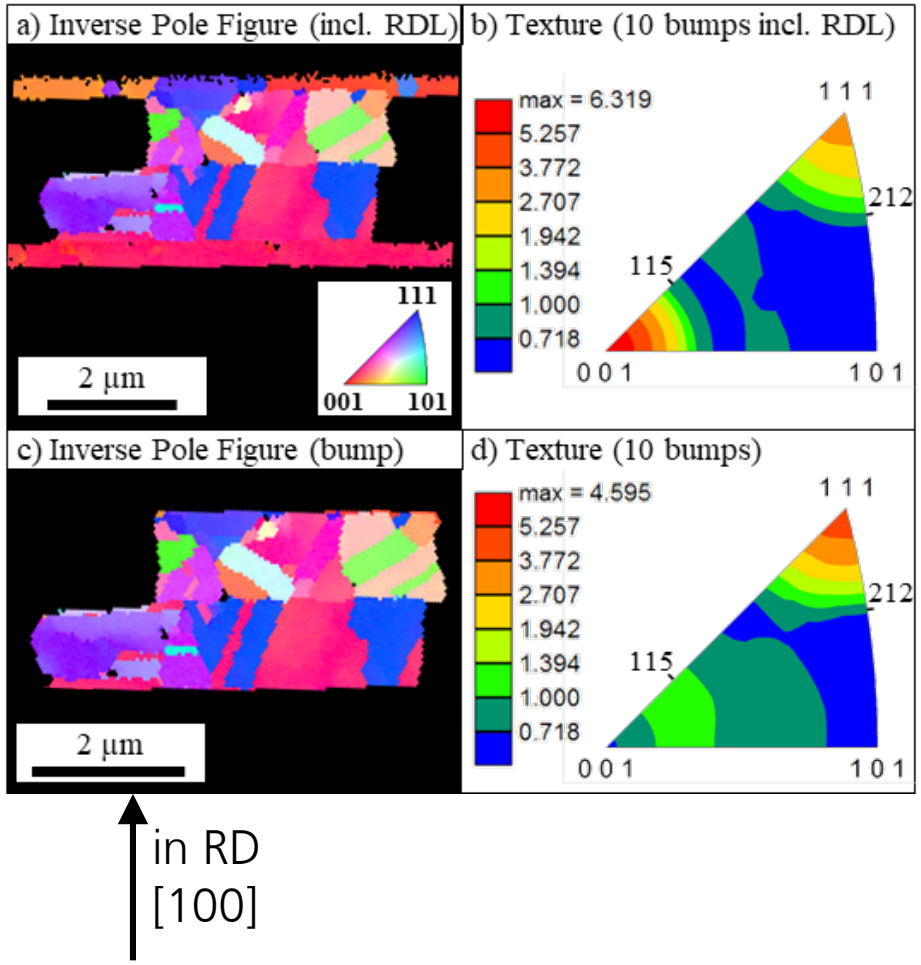
Hybrid bond interconnects

As bonded state: EBSD



Influence of underlying Cu-line on grain orientation (Texture):

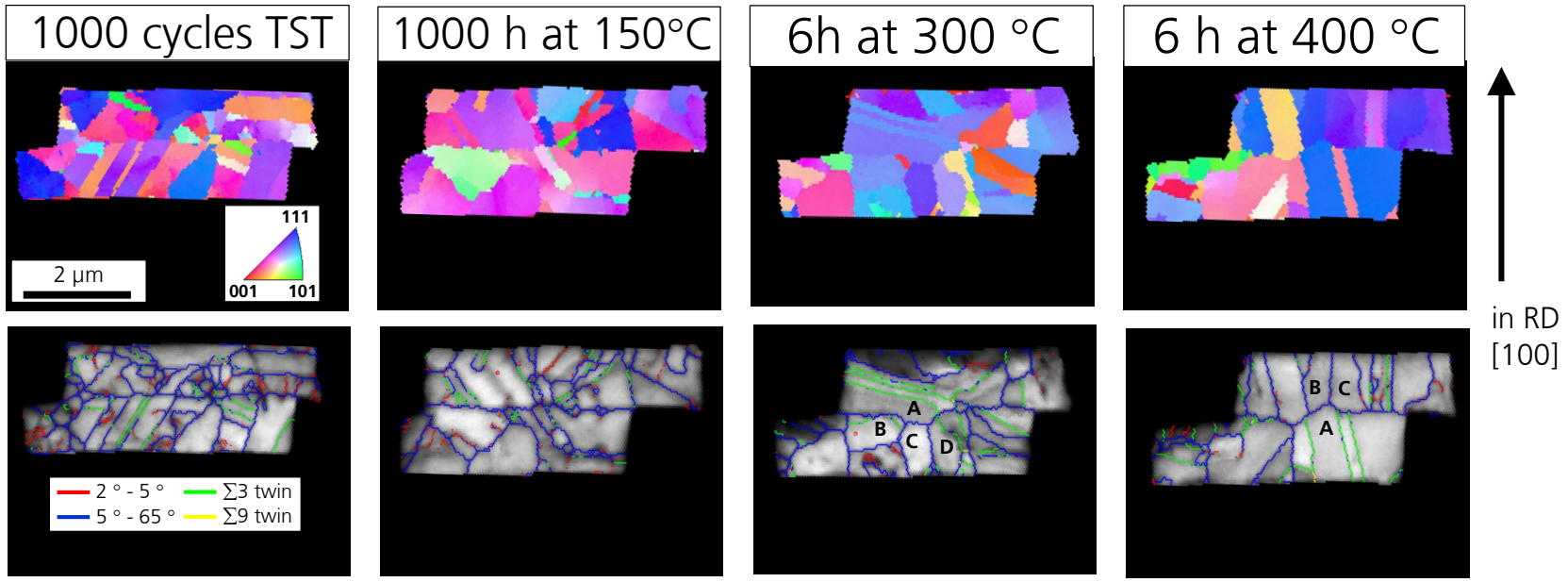
- analysis parallel to direction of Cu deposition (RD [100])
- underlying Cu-Line (PVD) shows strong {100} texture (twin → (212))
- Cu-bump (ECD) shows {111} texture (twin → (115))

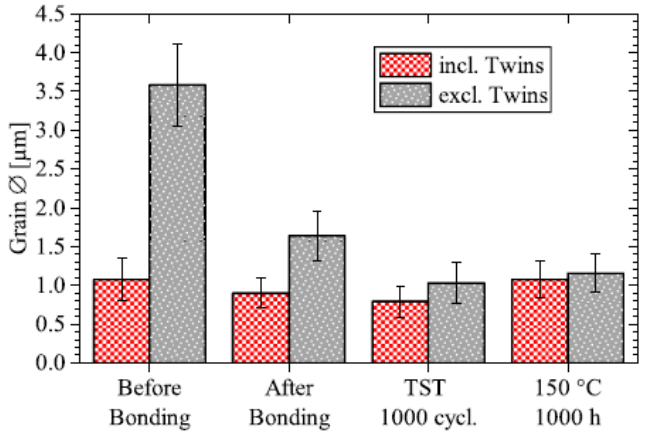
→ Bump structure was cut prior to texture analysis in order to eliminate the influence of the Cu-Line on the grain analysis result

Ref.: Panchenko I., IEEE trans., 2022

Hybrid bond interconnects

EBSD after reliability tests





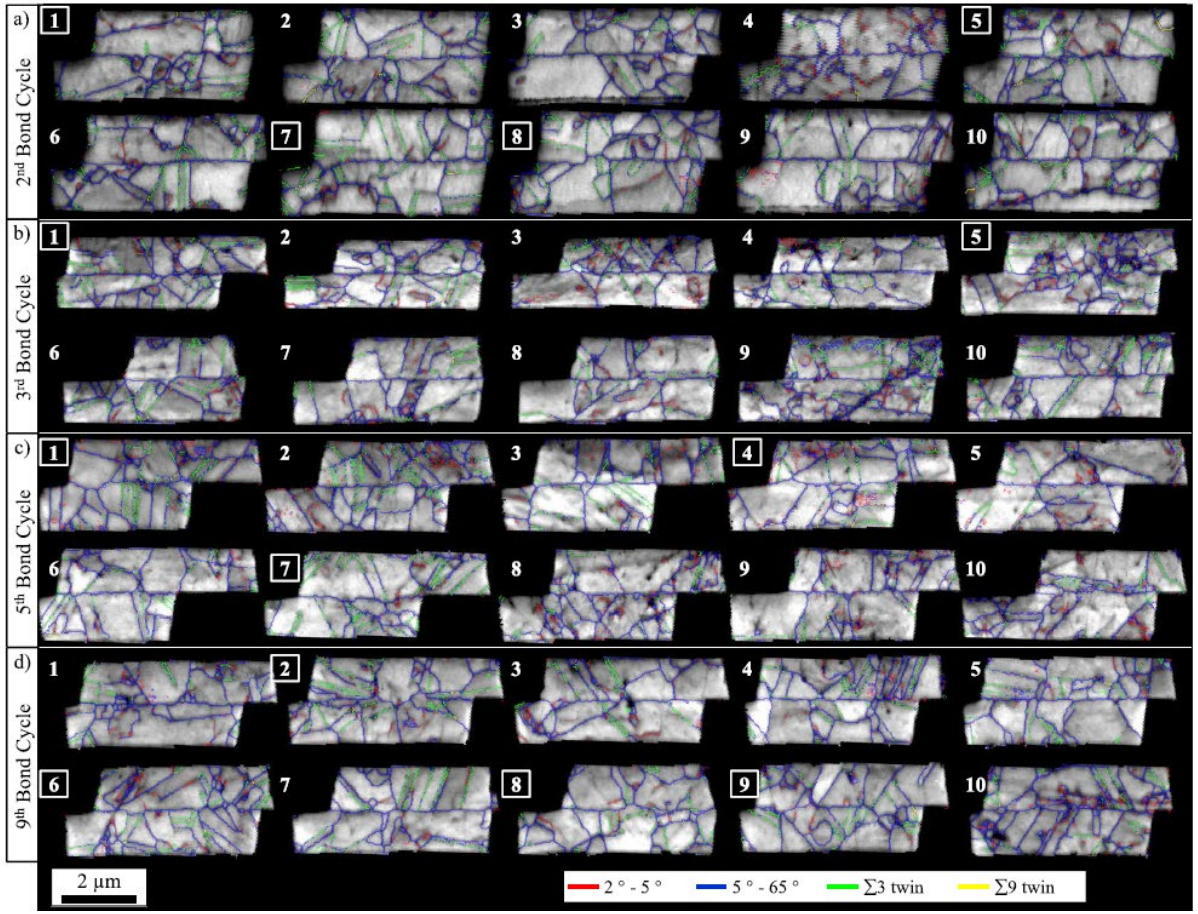
Average grain diameter and empiric standard deviation

- EBSD method allows detection of Cu grain intergrowth at interface (increased roughness)
- especially after storage at 300 and 400 °C (for some interconnects already visible after 0.5 h of storage)
- Grain growth at triple points

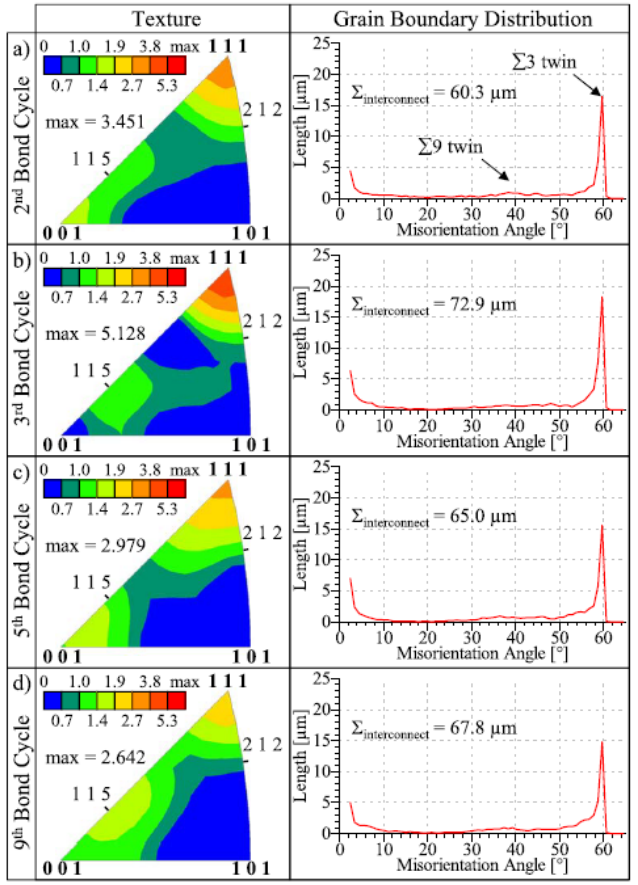
Ref.: Panchenko I., IEEE trans., 2022

Hybrid bond interconnects

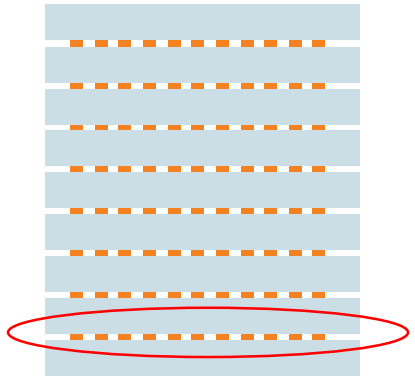
Multiple bonding cycles



Grain boundary map for all measured interconnects after multiple bonding cycles



Texture (planes parallel to the bonding interface)



- 9 bonding cycles for one W2W pair
- No defects after 9 bonding cycles
- texture {111} (and {115})

Ref.: Panchenko I., IEEE trans., 2022

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nanowired connects...

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Cu nanowired bump interconnect

Motivation

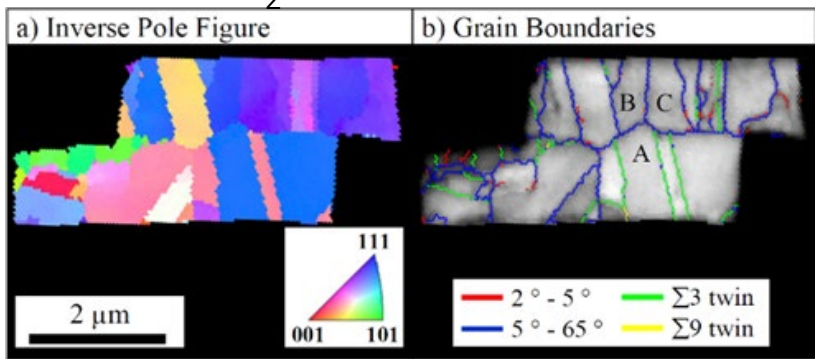
Why is the hybrid bond (or DBI) not always a right solution?

DBI-IP (XPERI)

Planarity, roughness

Sophisticated CMP demands

Cu/SiO_2 DBI – EBSD results



design impacts unknown

high annealing temperatures & times

Surface activation and cleaning

Very low contamination levels

Dicing challenges

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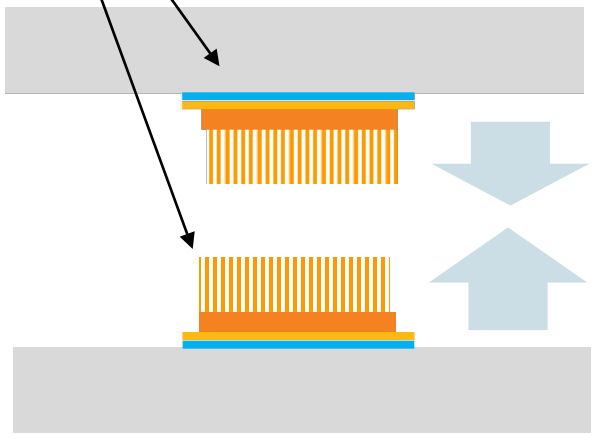
Nanowired Cu interconnect

Principles

Nanowired bump

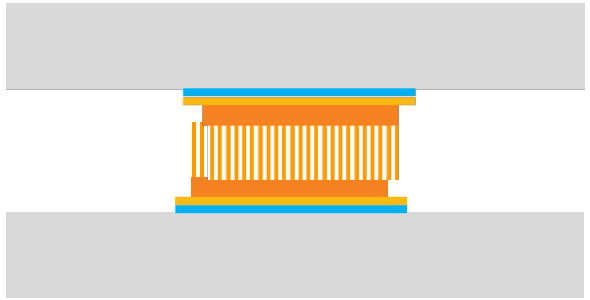


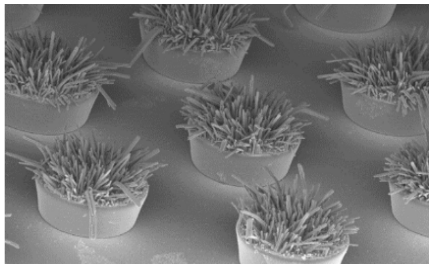
D2D Bonding:

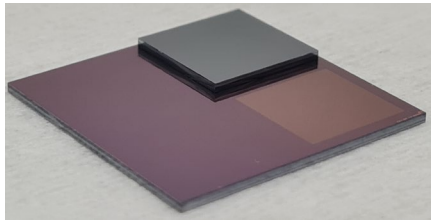
- T ~ 25°C
- Middle bonding pressure
- In air

Annealing for better performance

T ~ 150 … 300 °C







Advantages:

- Alternative for solder bump and Hybrid bond
- Only one metal
- Room temperature bond process
- Flux-free (clean of wires is still required)
- No complex design restrictions
- Low pressure bond is possible

Challenges:

- Oxidation of Cu Nanowires
- More process steps (membran, seed etch)
- Seed etch process need to be optimized
- Outgrowth of nanowires can cause shorts
- Limitations at miniaturization level (ø3µm?)
- Improval of mechanical strength

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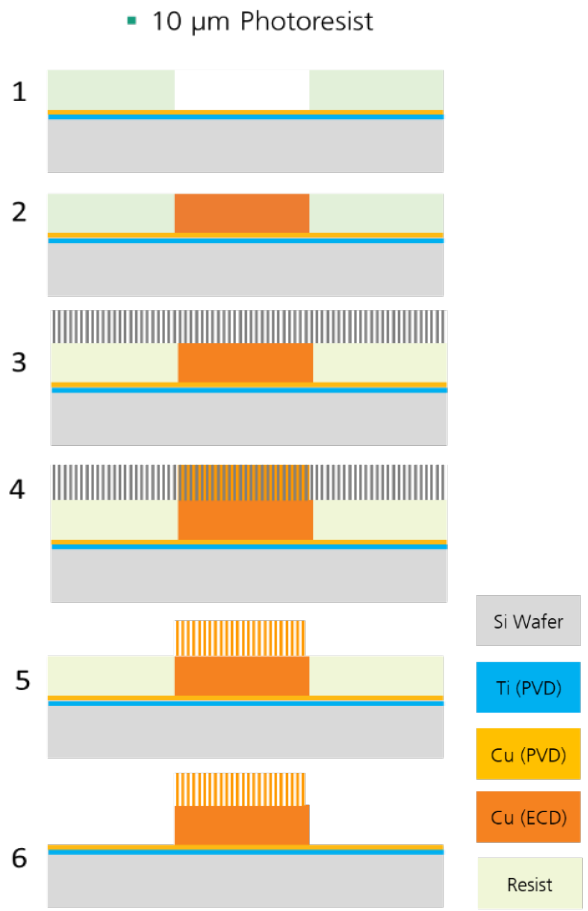
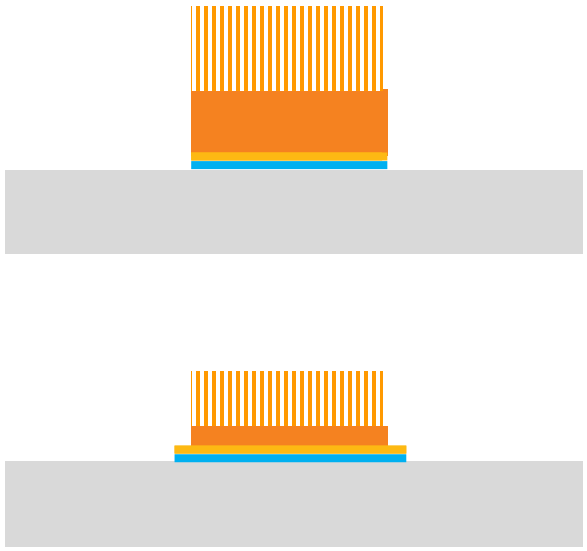
Nanowired Cu Interconnect

Processing of NW bump





Cu nanowired bump with base

- 10µm photoresist
- Ø 25 µm at 55 µm pitch
- ~ 10 µm of Cu base + 4 µm NW
- NWs with 200 and 400 nm

Cu nanowired bump without base

- 1µm photoresist
- < Ø 10 µm at < 55 µm pitch
- ~ 1 µm of Cu base + 5 µm NW
- NWs with 200 and 400 nm

! Both processes (with and without base) need alternative approach for Cu seed removal, because this influences the NW thickness !

- standard bump process is wet etch for barrier and seed
- NWs dissappears after wet etch due to nm thickness
- we have evaluated an alternative appoach with NW protection

Iuliana Panchenko et al., Hybrid bond and nanowired bump technologies for high density interconnect formation on wafer level

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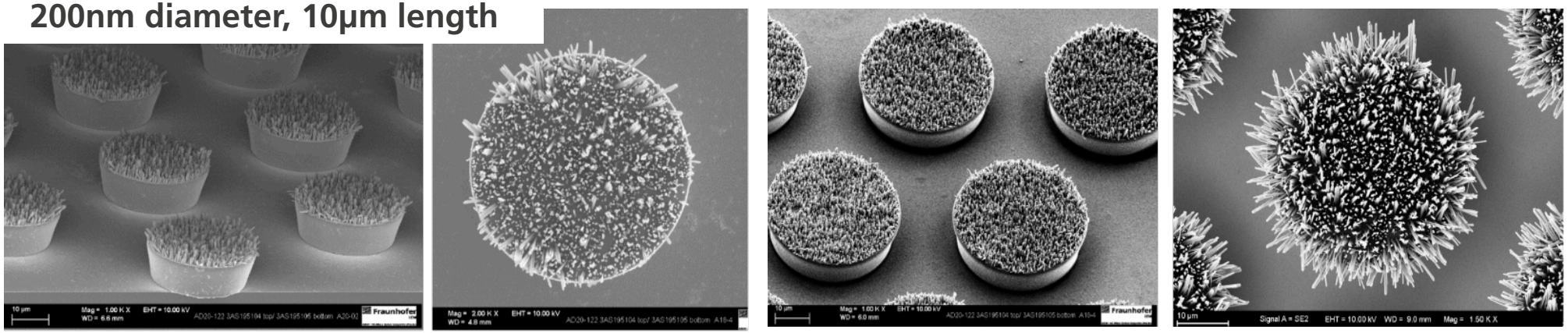
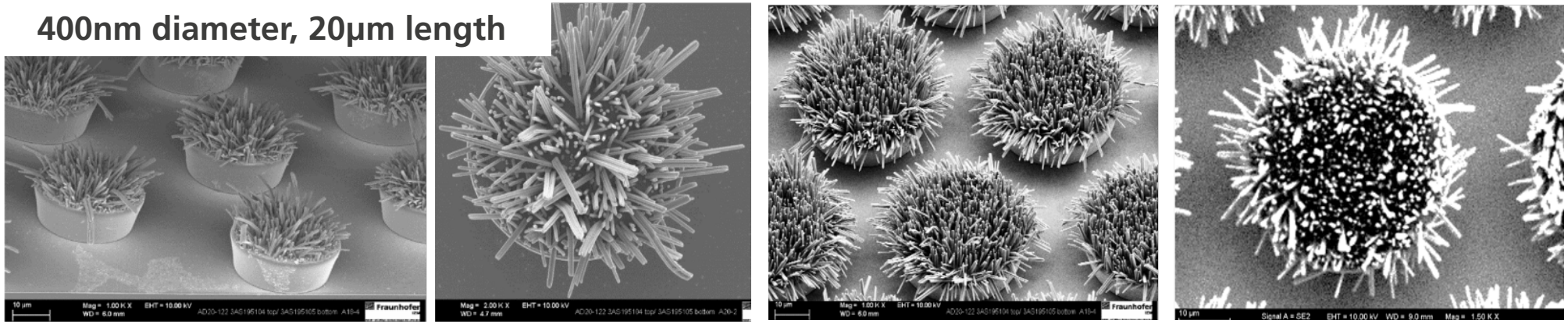
Nanowired Cu Interconnect

Morphology for 200 and 400 nm NWs

200nm diameter, 10µm length



400nm diameter, 20µm length



outgrowth

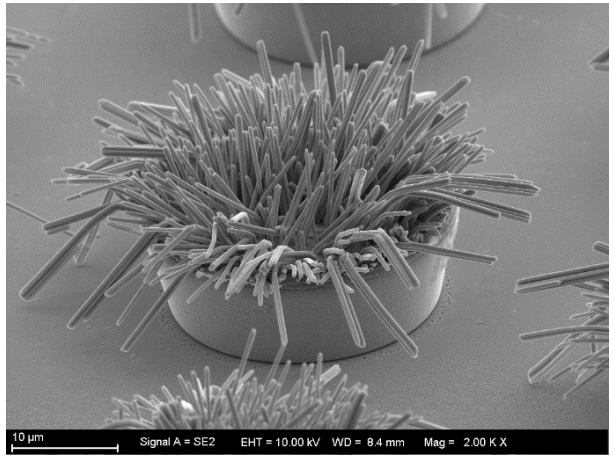
200 nm and less height is more stable against outgrowth
Current applications use approx. 5 µm height

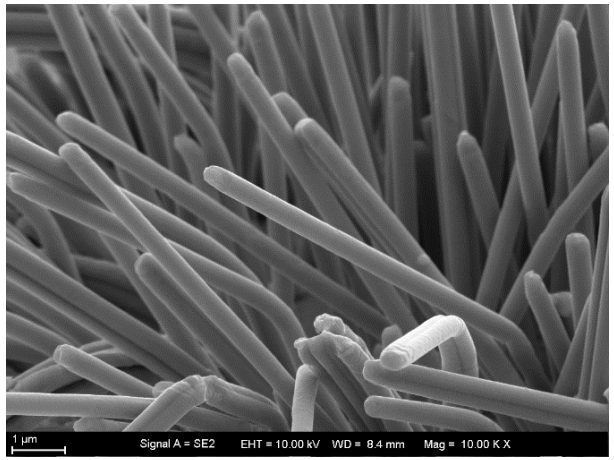
Ref.: Shehzad, ESTC, 2022

Nanowired bump interconnect

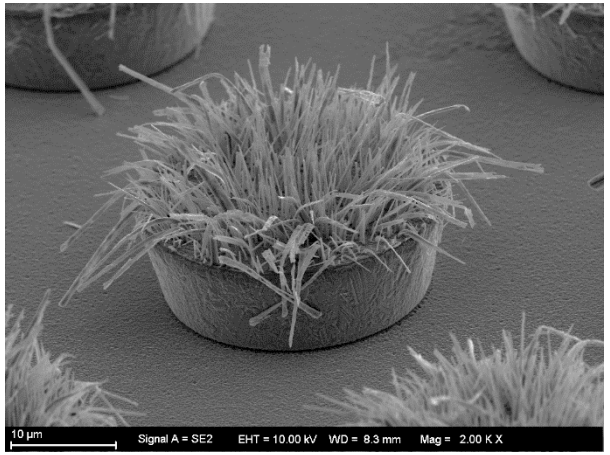
Removal of the Cu seed on wafer (manual test)

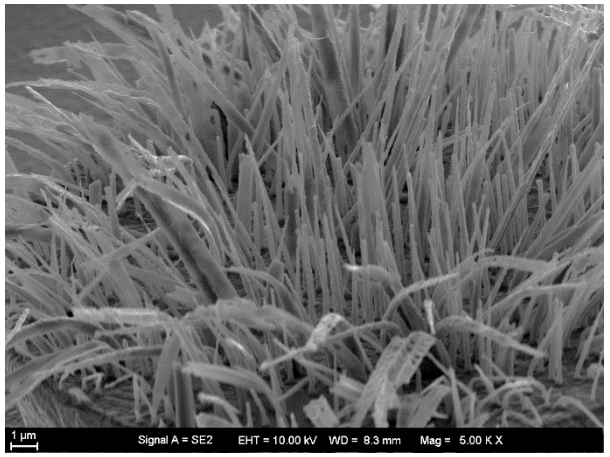
As plated



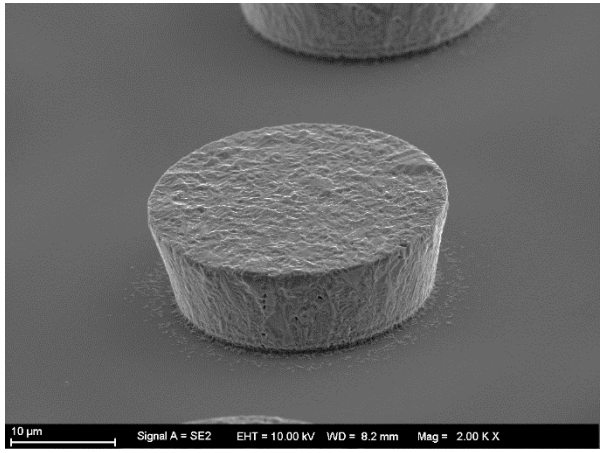


30 s wet etch





60 s wet etch



- All nanowires are completely removed after 60s
- Only after 60s fast completed seed removal at whole wafer

→ Alternative approach with NW protection for all new samples

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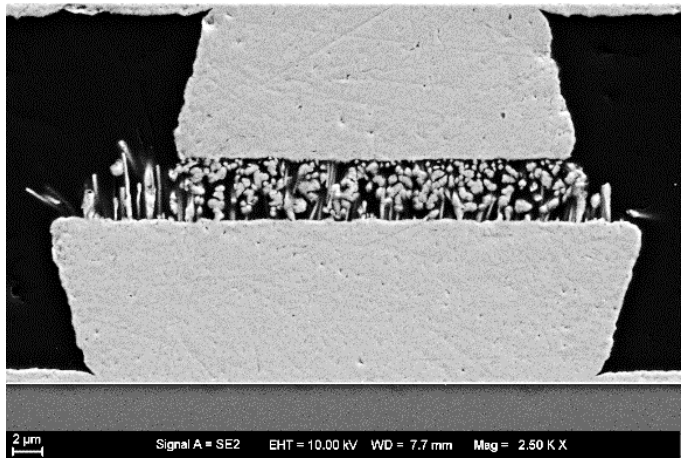
Nanowired bump interconnect

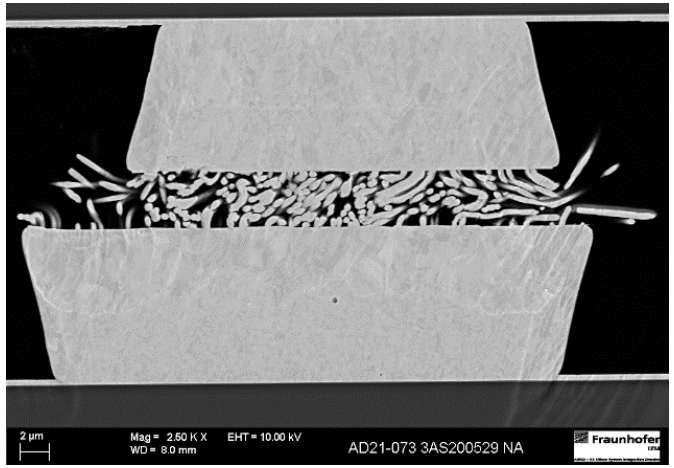
Influence of the bonding pressure (P)

P ~ 15 MPa

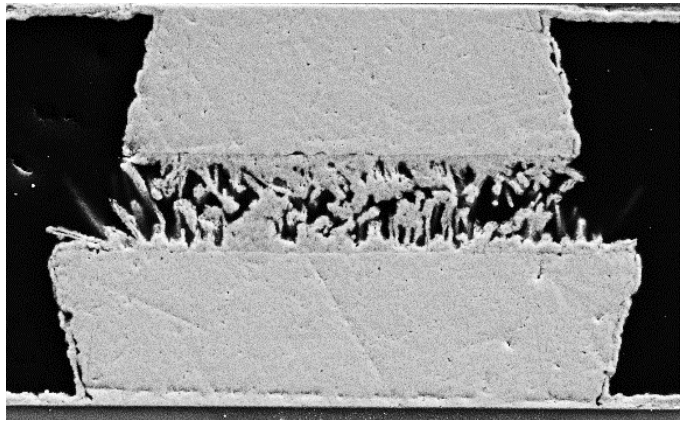
P ~ 80 MPa



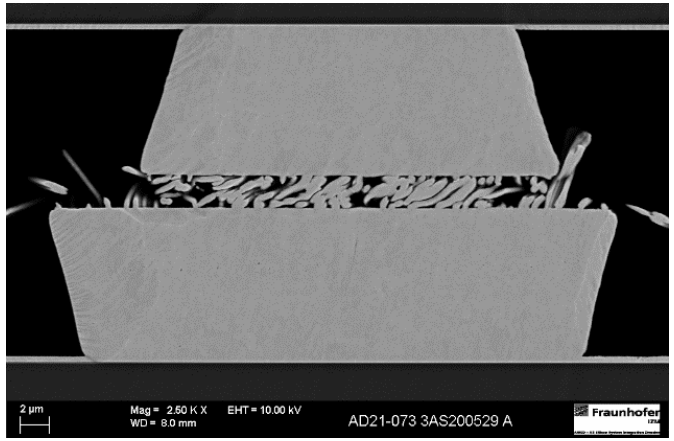
After bond at room T



- Almost no difference in microstructure
- P higher → shear strength higher
- Bond in air



After anneal 1h 300..350 °C



- Microstructure more compact
- Anneal → shear strength higher
- Anneal in N_2 atmosphere

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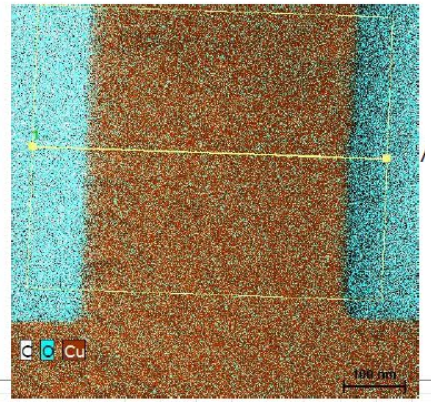
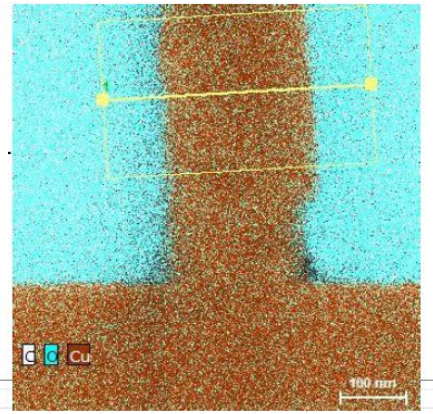
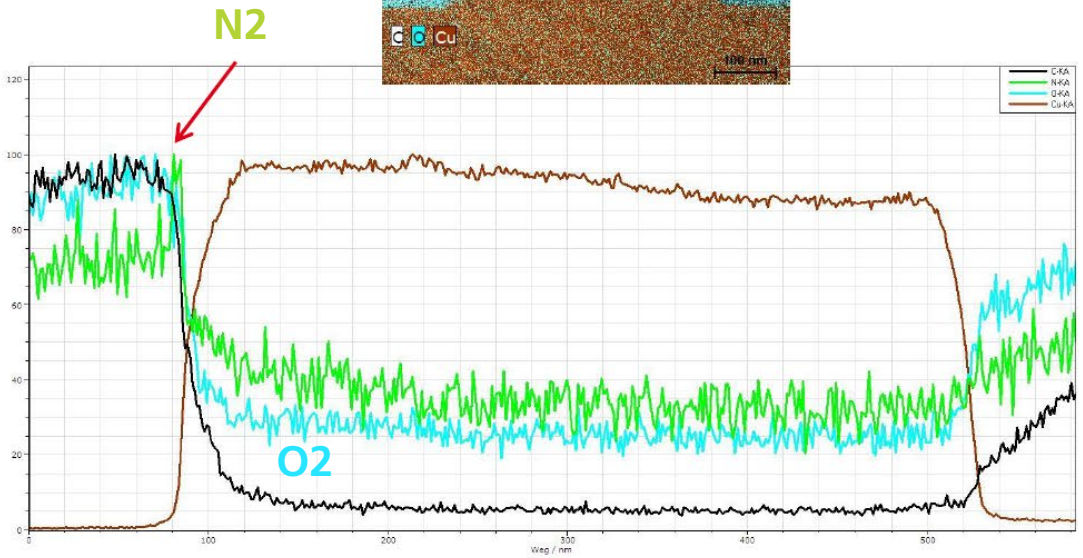
Nanowired bump interconnect

STEM investigation of the NWs as plated

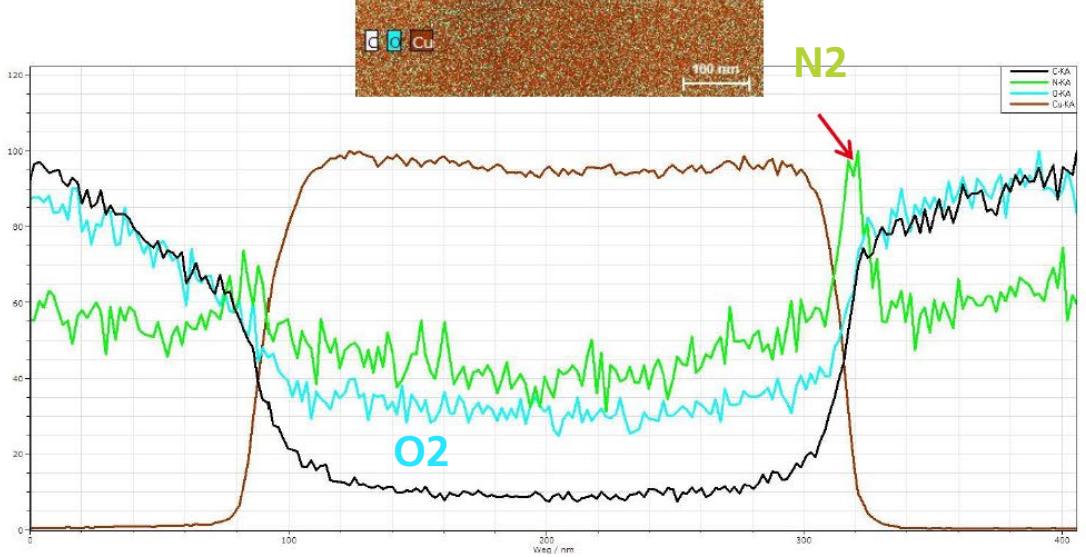
- More N_2 on the NW surface
- No explicit O_2 peak on NW surface







- 400 nm nanowires



- 200 nm nanowires

Nanowired bump interconnect

O_2 rich areas around the nanowires after bonding

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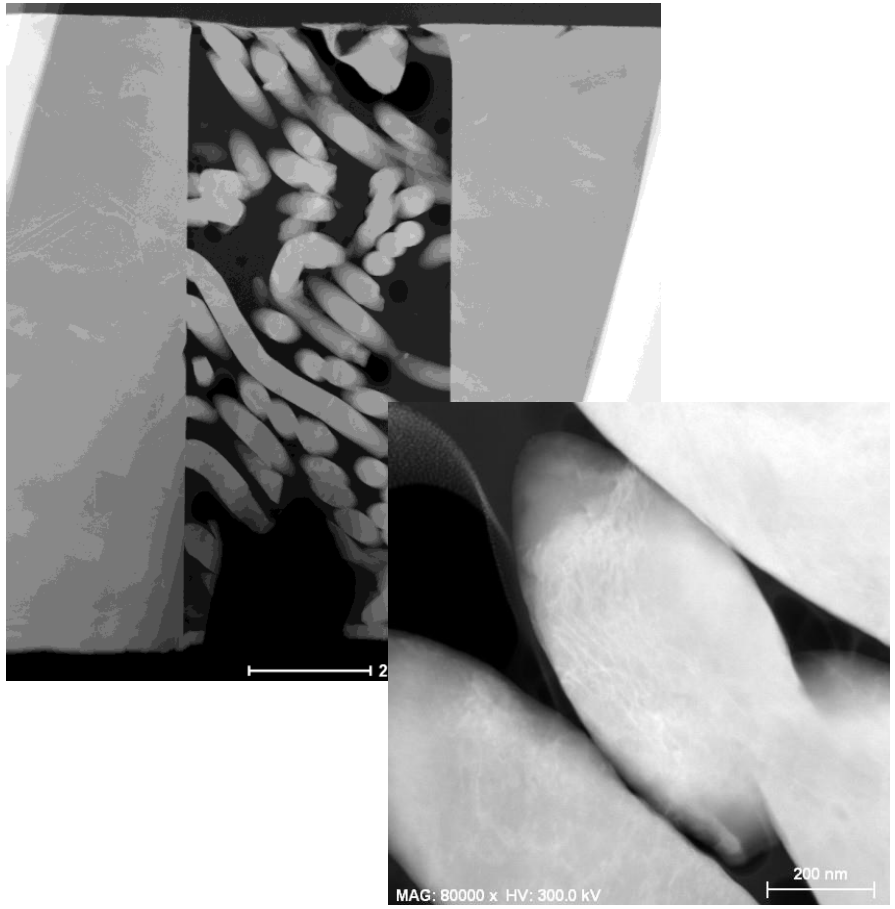
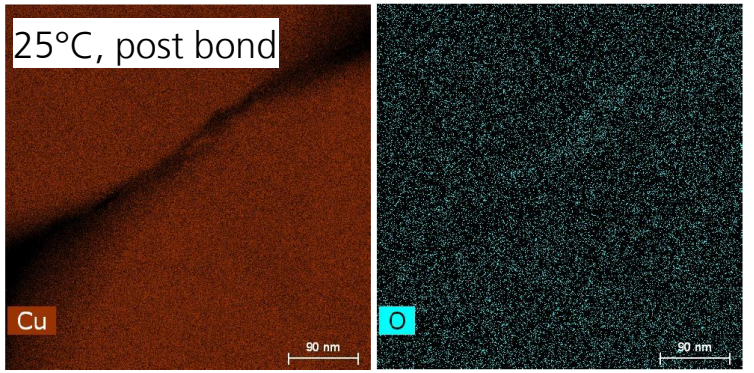
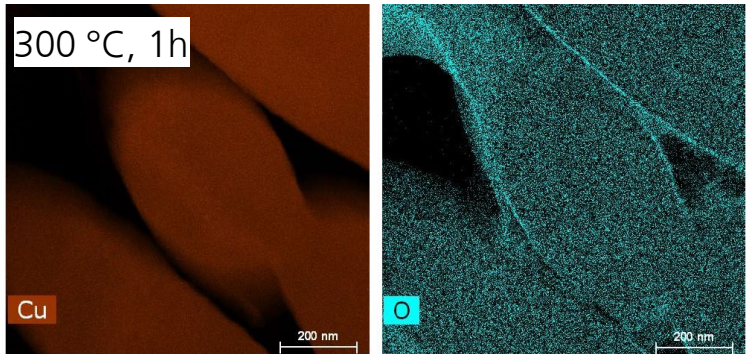
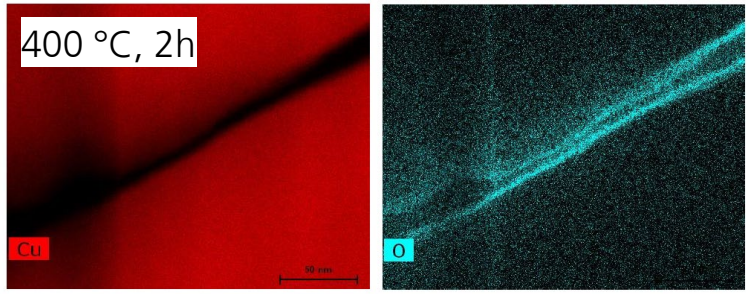
TEM lamella









More O_2 rich areas after longer anneal or higher T

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Nanowired bump interconnect

EBSD investigation of the NW microstructure

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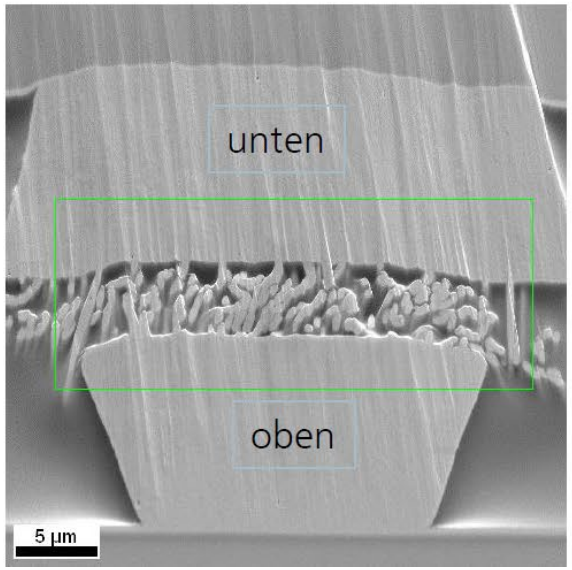
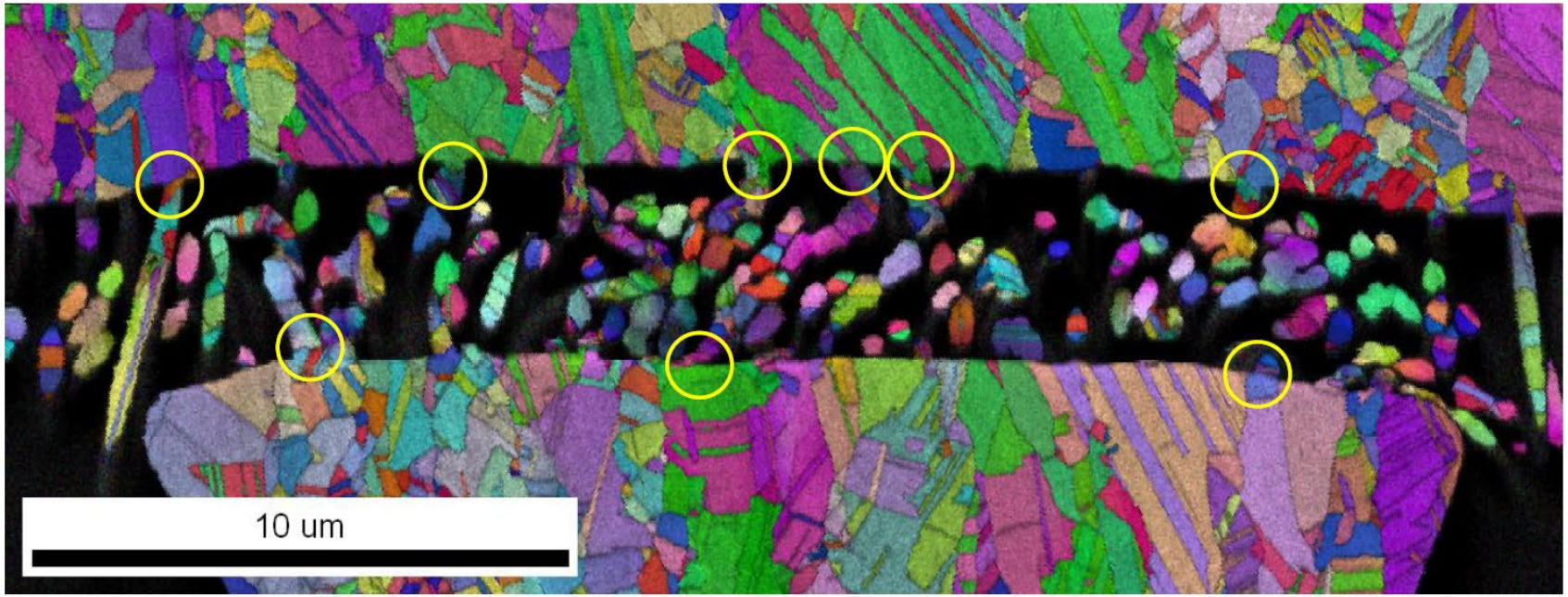
- Sample bonded and annealed
- FIB cut for preparation
- Only a small amount of NWs in cut plane, all appear in different directions
- NWs have most probably lammelar grains and follow the orientation of the underlying Cu base bump





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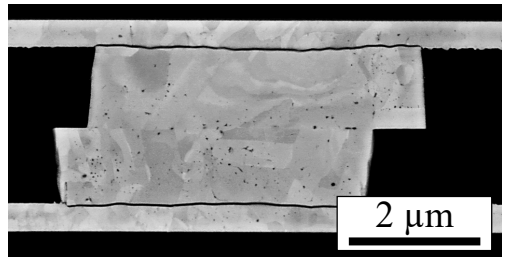
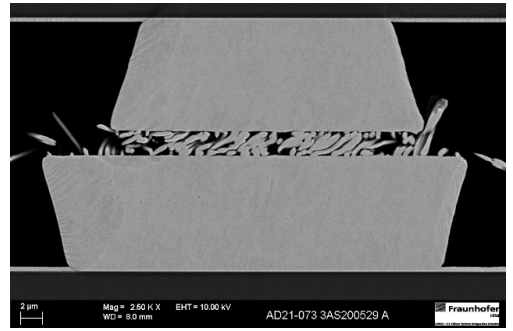
Summary and outlook

- An overview of the fine-pitch interconnect technologies was presented, special details for hybrid bond and nanowired bump interconnect were discussed
- Hybrid bond technology is an interconnect of choice by now due to excessive miniaturization possibility and high reliability for W2W and D2W/D2D
- An alternative for hybrid bond is nanowired bump, which does not suffer from the design impact, does not need challenging CMP and can be used for room T bonding
- Detailed study of microstructure (TEM, EBSD, SEM) were shown for both technologies
- Further investigations are needed for electrical characterization of nanowired interconnects, Cu activation and nanowire integration scheme in complex interposer flows, as well as combination of pad sizes for hybrid and nanowire





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Acknowledgement

Ms. Ran Yin (TU Dresden)

Mr. Akash Mistry (TU Dresden)

Anke Hanisch (previous FhG IZM ASSID)

Colleagues from PFA lab at IAVT TU Dresden, FhG IZM ASSID (J. Krause) and at FhG IMWS

All colleagues from clean room processing FhG IZM ASSID

All colleagues from lab processing at Nanowired GmbH

Financial support by: “Functional Integration for Micro-/Nano-Electronics” under Grant 100245395 and Grant 100249378 and “Transfer center: Functional Integration for the Micro-/Nano-Electronics” under Grant 100368159 and Grant 100368161, “Wafer Metrology Center” EU project 16ME0057, “NanoInt” Fraunhofer SME internal project.

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Thank you!

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